COMPARATIVE STUDY OF SYNCHRONIZER CIRCUITS

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May 9, 2016
OUTLINE OF PRESENTATION

- Synchronizer Circuits
- Analysis of three synchronizer circuits using small-signal modeling
- Comparison with simulations
- Comparison with experimental data
- Summary and conclusions
OBJECTIVE OF THIS WORK

- Mean time between failure (MTBF)

\[ MTBF = \frac{e^{\frac{t_a}{\tau}}}{T_\omega \cdot f_c \cdot f_d} \]

Synchronizer circuit

Technology scaling

PVT Variations

Effect of synchronizer circuit design, technology scaling and process variations in \( \tau \) and MTBF: Analysis, Simulations, Experiments

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ASYNC 2016
SYNCHRONIZER CIRCUITS : STANDARD DFF

Standard cell library component
S. Yang, I.W. Jones and M. Greenstreet, “Synchronizer performance in deep sub-micron technology,” ASYNC 2011
SYNCHRONIZER CIRCUITS: JAMB LATCH

ANALYTICAL MODELS: STANDARD FF

ron1, rop1, i1n, i1p : Correspond to path 1
ron2, rop2, i2n, i2p : Correspond to path 2
APPROXIMATION AND SIMPLIFICATION

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Small-Signal Analysis

\[ G_{m1}v_2 + C_1 \frac{dv_1}{dt} = 0 \]

\[ G_{m2}v_1 + C_2 \frac{dv_2}{dt} = 0 \]

\[ v_1(t) = v_m \exp\left(\frac{t}{\tau}\right) \quad \tau = \frac{\sqrt{C_1 C_2}}{\sqrt{G_{m1} G_{m2}}} \]

\[ G_{m1} = g_{mn} + g_{mp} \]

\[ G_{m1} = \left( \mu_n c_{oxx} \frac{N5}{L} \cdot \frac{1}{1 + \sqrt{a}} + \mu_p c_{oxx} \frac{P5}{L} \cdot \frac{a}{1 + \sqrt{a}} \right) (V_m - |v_{tp}| - v_{tn}) \]

\[ a = \frac{\mu_n c_{oxx} N5}{\mu_p c_{oxx} P5} \frac{L}{L} \]
ANALYTICAL PLOTS

- Across different technology nodes: 180nm, 130nm, 90nm, 65nm
- Across multiple process corners: FF, SS, TT, SNFP, FNSP
- For 3 different synchronizer circuits
ANALYTICAL PLOTS

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SIMULATION STUDY
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SUMMARY AND OBSERVATIONS

- Comparison of 3 different synchronizer circuits
  - At 4 technology nodes (180nm, 130nm, 90nm, 65nm)
  - Over all the 5 process corners
  - Using both analytical models and simulations

- Observations
  - Analytical models follows the simulation trends
  - Technology scaling observed in Simulations/Analysis different in Experiments (but more study required)
  - Pseudo-NMOS is more resilient to process variations (and scales better with technology!)
THANK YOU