More Moore or More Than Moore?

Raj Jammy  PhD
VP, Materials and Emerging Technologies
SEMATECH
Contents

• Overview
• Industry trends
• CMOS (More Moore) options
• Beyond CMOS (More than Moore) options
• Conclusions
Overview

- **More Moore**: Scaling as per Moore’s Law
  - Double number of transistors every ~two years
  - Challenges:
    - Unsustainable power dissipation
    - Atomic scale dimensions- physical limits
    - Process and device variability
    - No real performance increase with scaling
    - Expensive R&D and manufacturing costs

- **More than Moore**: Application driven components
  - Analog, RF, M(N)EMS, sensors, opto, power devices,..
  - Challenges:
    - Bulky
    - Incompatible with CMOS
    - Often unsuitable for mobile platforms

*To get More from Moore, More than Moore is a must!*
How is the industry changing?

1) Mobile trend – performance AND power critical

- Mobile products have increased share of the Semiconductor TAM
- IMPACT: Need low power device, sensing(analog), storage, display solutions
How is the industry changing?

2) Data center trend; performance AND power critical

Data centers in the United States alone soaked up about 61 billion kilowatt-hours (kWh), or $4.5 billion worth of electricity in 2006. If current energy usage trends continue, a U.S. Environmental Protection Agency predicts U.S. data centers will use more than 100 billion kWh by 2011, representing $7.4 billion in annual electricity costs and 2.5 percent of the nation’s total electricity.

- Cloud computing growing – logic & memory for data centers important!
- IMPACT: Dedicated power stations for data center ops and cooling (?)
- IMPACT: Data centers need **Both** Low Power & High Performance

Source: EIA, NREL May 2009
How is the industry changing?

3) SOC trend; performance AND power critical

- SOC requires combining digital, analog, passives and lots of memory
- IMPACT: Mainstream chips are no longer restricted to discrete memory or logic
- IMPACT: Memory needs to be low power too

**System-on-Chip Building Blocks**

**CPU vs. SoC Technology Comparison**

Differences
- Logic Transistors
- Precision Passives

<table>
<thead>
<tr>
<th></th>
<th>CPU</th>
<th>SoC</th>
</tr>
</thead>
<tbody>
<tr>
<td>High Speed</td>
<td>None</td>
<td>Low Leakage</td>
</tr>
<tr>
<td>R, C and L</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Source: Y. Nishi, S.M. Sze, EE319 Lecture Stanford 2009
How is the industry changing?

4) It is not just a digital world!; performance AND power critical

- Most “digital” consumer systems have significant
  - Analog and Communication components
  - Memory
  - Significant need for low power operation
Industry “must solve” challenges

- **Must Solve: Power-Performance Trend**
- **Must Solve: ExaFLOP / Terabit Power, $$$**

New materials, processes, tools, devices for next generation low power technologies

Chip makers/design houses will drive multi-core designs, circuit power optimization

<table>
<thead>
<tr>
<th>Enterprise Logic</th>
<th>Enterprise Memory</th>
</tr>
</thead>
<tbody>
<tr>
<td>TODAY</td>
<td>GOAL</td>
</tr>
<tr>
<td>Energy (per OP or bit)</td>
<td>1000pJ</td>
</tr>
<tr>
<td>Power Cost</td>
<td>$1B</td>
</tr>
</tbody>
</table>

Source: DARPA and Kryder, et. al. IEEE TRANS ON MAGNETICS, VOL. 45., OCT 09

Adapted from: Y. Nishi, S.M. Sze, EE319 Stanford 2009
Common theme

• GOAL: Device with low power AND high performance
• Avoid cost, complexity of dozens of devices on a chip
How to address “must solve” challenges?

Pareto analysis of power issue

How to address “must solve” challenges?

Pareto analysis of power issue

#1: Dynamic “leakage”

V_{dd} Scaling (Vdd=0.3-0.6V)

#2: Subthreshold Leakage

Junctions, damage, TFET

30%

#3: Gate Leakage

HK/MG

20%

For V_{dd} Scaling, Transistors Need:

- Good mobility [strain, Ge, III-V, etc…]
- Robust electrostatics [scaled HK/MG, USJ, finFETs, nanowire FETs, …]
- Controlled stochastics /variability [t_{si} in SOI, low R_{con} materials, fin LER …]
Power performance trade-offs

More Moore opportunities

- High Mobility materials
  - SiGe, Ge, InGaAs

- Better electrostatic control
  - Multiple gates + more channel area
  - FinFETs, nanowire FET
  - Low $T_{inv}$: Scaled HKMG
  - USJ
  - Parasitics ($R_{co}$, $C_p$..)
Gate stack plays critical role in roadmap

- Zero Interface Layer HK reduces Jg by $10^7 \times$
- 2nd and 3rd generation HKMG will also require ZIL
Ultra shallow junctions
Scaled USJ: conventional and damage-free

- Standard implantation
- Flash anneal
- Rs~1050-1100Ω/sq
- "Monolayer" doping
- Low Rs & damage free
- Suitable for group IV & III-V

Xj ~7.5nm
Contacts: Key scaling challenge

Schottky Barrier height engineering to lower Rc

- 600 – 800 meV tuning of Schottky Barrier Height
- N and P-Si contact engineering for conventional Ni based dual silicides
- Potential dual silicide solution for nodes well beyond 16nm
- Simple and manufacturable approaches – help low power operation

MOSFET scaling

Rc Reduction in NiSi: Three Methods

• Reverse Bias IV Measurement
• Depletion CV Measurement

Si Bandgap vs. \( t_{\text{High-}\kappa} \) (A)

B.Coss et al VLSI 2009 5B
WY Loh et al VLSI 2009 5B
Transistor performance improvement

Lower $R_{ext}$

- 24% enhancement in drive current for doped NiSi DSS-nFETs

$V - V_T = 1.0V$

B. Coss et al. VLSI 2009 5B
WY Loh et al. VLSI 2009 5B
High mobility channels: Quantum-well MOSFETs
Short channel Planar Si/SiGe/Si QW pFETs

- Best reported short Lg pFET (Ion/Ioff ~ $5 \times 10^4$) devices with high Ge%
- Defect-free thin SiGe, Ge PMOS for high performance application
- Better than state-of-art Si on power / performance metric
- No uniaxial strain in this work – further boost possible
- Demonstrated concept in scaled non-planar scheme as well as in III-V
Value of III-V
Performance @ Power

III-V demonstrated as superior to state-of-art Si in:
- Fundamental Energy to Switch
- Energy ⇔ Speed Benefits
- Energy*Delay Benefit w/ scaling
- Many issues to be resolved

Source: R. Chau et al., CSICS 2005
Properties of promising high mobility materials [electrons and holes]

\[ I_{dsat} = \mu \frac{A \varepsilon \varepsilon_o W}{T_{ox,inv} 2L} (V_{dd} - V_t)^2 \]

<table>
<thead>
<tr>
<th>Property/ Material</th>
<th>Si</th>
<th>Ge</th>
<th>GaAs</th>
<th>In(<em>{0.53})Ga(</em>{0.47})As</th>
<th>InAs</th>
<th>Graphene</th>
</tr>
</thead>
<tbody>
<tr>
<td>Eg (eV)</td>
<td>1.1</td>
<td>0.66</td>
<td>1.4</td>
<td>0.75</td>
<td>0.35</td>
<td>0*</td>
</tr>
<tr>
<td>(\mu_n) (cm(^2)/v-sec)</td>
<td>1,350</td>
<td>3,900</td>
<td>4,600</td>
<td>&gt;8,000</td>
<td>40,000</td>
<td>&gt;100,000</td>
</tr>
<tr>
<td>(\mu_p) (cm(^2)/v-sec)</td>
<td>480</td>
<td>1,900</td>
<td>500</td>
<td>350</td>
<td>&lt;500</td>
<td>&gt;100,000</td>
</tr>
<tr>
<td>(m*/m_o)</td>
<td>0.165</td>
<td>0.12</td>
<td>0.067</td>
<td>0.041</td>
<td>0.024</td>
<td>&lt;0.01</td>
</tr>
<tr>
<td>Lattice mismatch to Si</td>
<td>0</td>
<td>4%</td>
<td>4%</td>
<td>8%</td>
<td>12%</td>
<td>n.A</td>
</tr>
</tbody>
</table>

* Tunable but at cost of \(\mu\) degradation

pMOSFET  nMOSFET
III-V/Si for VLSI using 200 mm line

- 1st ever demonstrated flow for III-V on Si FETs using industry standard tool set
- Systematic materials evaluation/process development for industry infrastructure
Non-planar devices: FinFETS and nanowires

- 6-8 nm Fins
- Dual Channel Fin FET
- Fin FETs
- Nanowire FETs

<table>
<thead>
<tr>
<th>Platform</th>
<th>Wafer Types</th>
<th>FinFETs</th>
<th>Nanowires</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Bulk</td>
<td>2 Gates</td>
<td>Single wire</td>
</tr>
<tr>
<td></td>
<td>SOI</td>
<td>3 Gates</td>
<td>Stacked wires</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Tall Fins</td>
<td>High Mobility Channel</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Heterogeneous Fin Channel</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Single wire</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Stacked wires</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>High Mobility Channel</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Heterogeneous Wire Channel</td>
</tr>
</tbody>
</table>

- Lg \sim 30nm
- V_{TH} = -0.52V
- DIBL = 60mV/V
- SS = 67mV/dec
- EOT \sim 1nm

- Lg \sim 30nm
- V_{TH} = 0.26V
- DIBL = 49mV/V
- SS = 70mV/dec
- EOT \sim 1nm

- SNM of 300mV

- SRAM

- 6-8 nm Fins
- SEMATECH Si Nanowire
- SiGe
- Si

- FinFETs Nanowires Wafers
Non-planar device scaling

Scaling Pathways

w and w/o 3rd gate?

Bulk vs SOI

High $\mu$ and w/o 3rd gate?

Homogeneous

Heterogeneous

High $\mu$

OR

OR

Model based understanding using simulation + experimental data.

Trigate 40nm*10nm

Nanowire 10nm*10nm

QW Volume Inversion

FinFET with Heterogenous Channel

20nm

SiGe(100)

Si(100)

InGaAs

Si

SiGe

45%
FinFETs with SiGe and SiGe/Si Fins

(110) fin sidewall surface. Current in <110> direction.

(100) fin sidewall surface. Current in <100> direction.

SiGe channel shows significant improvement over Si control (no intentional strain in these devices)
Si nanowire arrays/stacks

Single Si NW FETs

Stacked NWs

Si/SiGe High $\mu$ Nanowire
Voltage scaling

Device Research Roadmap

Achieving energy efficiency by aggressively reducing operating voltage

- "High inversion charge"
  - Poly SiON
  - Metal High-k
  - Si Substrate

- "Superior electrostatics"

- "High carrier velocity at low E-field"
  - High \( \mu \) quantum well
  - III-V, Ge, Graphene materials

- "High \( I_{on} \) to \( I_{off} \) over limited swing"

- "Interconnectless passive transmission"

- Sub 100 mV Sub 0.25 V Sub 0.5 V Sub 0.8 V Sub 1.0 V

- 2005 65nm
- 2007 45nm
- 2009 32nm
- 2011 22nm
- 2013 15nm
- 2015 10nm
- 2017 7nm

S. Datta
Pathways for low power CMOS & beyond…

Disruptive Gate Stacks and Dual WF Metal Gates for LP/HP

Graphene

TFETs

NEMS

High $\mu$ Channel Materials

Gate-First nMOSFET 700°C anneal

Low R Contacts

Contact through ILD

Spacer

Si fin (~10nm wide)

Gate-First nMOSFET 700°C anneal

Gate

Source

Drain

Damage-free Junctions

Channel Structures

Numerous Options …breakthroughs needed, but exciting possibilities
Power performance trade-offs
More than Moore opportunities

- High Mobility materials
  - SiGe, Ge, InGaAs
  - Graphene [$\mu_e \approx 15000 \text{ cm}^2/\text{V-s at RT}$]

- Better electrostatic control
  - Multiple gates + more channel area
  - FinFETs, nanowire FET

- Improve on-off ratio
  - Tunnel FET
    - Very steep $\Delta V_{SS} << 60 \text{ mV/dec}$
    - Low bias voltages ($<< 1 \text{V}$)
  - Nano Electro Mechanical switch (NEMS)
    - Hybrid: $I_{on}$ by CMOS + $I_{off}$ by NEMS
    - Zero Leakage Power
Schottky-source tunneling FET

Sub-60mV/dec subthreshold swing
Conventional Si CMOS limit: 62mV/dec

- New device concept: Schottky Source TFET with SS ~ 46mV/dec

With UC Berkeley
# NEMS: Nano Electro-Mechanical Switch

<table>
<thead>
<tr>
<th></th>
<th>MEMS</th>
<th>NEMS</th>
<th>Gain</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency</td>
<td>kHz</td>
<td>GHz</td>
<td>Ultra low power</td>
</tr>
<tr>
<td>Power</td>
<td>mW−μW</td>
<td>pW</td>
<td>Faster operation</td>
</tr>
<tr>
<td>Quality factor</td>
<td>$10^7$</td>
<td>$10^4$</td>
<td>Challenge</td>
</tr>
<tr>
<td>Sensitivity</td>
<td>High</td>
<td>Highest</td>
<td>High sensitivity</td>
</tr>
</tbody>
</table>

Dadgour et al, Session 1.1.1, ISLPED 2010  
M. Hussain et al, NATO Nano DSA, 2009
MEMS/NEMS “zero leakage” devices

Disruptive memory/logic switch

Why NEMS Memory?

- NEMS may get to 6F² [1,2]

Why NEMS Memory?

- NEMS may get to 6F² [1,2]

Current (μA)

Voltage (V)

Hysteresis window ~5V

Vπ = 4.25V

NEMS NAND

Before initialization

- \( A \) = 1, \( B \) = 0 → \( \text{out} = 1 \)
- \( A \) = 1, \( B \) = 1 → \( \text{out} = 0 \)
- \( A \) = 0, \( B \) = 0 → \( \text{out} = AB \)

Once the beam is pulled-in, \( VDD > Vpi \) is no more needed to hold the beam, \( VDD > Vpo \) is sufficient

Comparison for the same delay (10.5 ns) and realistic dimensions

\[ V_{DD} = 2.24 \text{ V} \] (Conventional)
\[ V_{DD} = 0.59 \text{ V} \] (Energy-Reversible)
NEM switch fabrication

- CMOS Compatible NEMS
- Can be integrated easily with conventional CMOS for logic/memory/sensing
NEMS-based logic circuits

Inverter Gate

XOR/XNOR Gates

Alternative implementations of XOR/XNOR gates

Hamed Dadgour et al, ISLPED 2010

AND Gates

- NEMS relay outperforms conventional relay in terms of energy, voltage and reliability

100mV switching is possible with few nanometers gap

The implementation of a two-input AND gate
NEMS: Robust, CMOS compatible, nanoscale switch

- Potential on-the fly impedance matching for analog/mixed signal applications
- Versatile device platform: the “transistor” of the MEMS world

**Basic Building Block**
- Well studied
- Highly manufacturable
- Extremely versatile
- Scaling friendly → higher sensitivity, lower cost, powerful arrays

**Example: in-situ process monitoring**
- Capacitance Sensor
- Resistance Sensor
- Temperature Sensor
- Pressure Sensor

- CMOS
- Analog

- + Well studied
- + Highly manufacturable
- + Extremely versatile
- + Scaling friendly → higher sensitivity, lower cost, powerful arrays
Optimized low VCC MIM stack for Analog/MS

- Meets ITRS specs to 2013 for analog and mixed signal needs
- Robust manufacturing ready process
### Analog mixed signal

**Passive components development**

<table>
<thead>
<tr>
<th>Component</th>
<th>Structure</th>
<th>Issue(s)</th>
<th>Approach</th>
<th>SEMATECH Contribution</th>
</tr>
</thead>
</table>
| Varactor  | ![Varactor Diagram] | • Linearity  
• Area scaling (cap/µm²) | • Abrupt Junction  
• Barrier Height Reduction @ M-S contact  
• ↓ Parasitic R | • Dipole tuning SBH  
• N Implant tuning SBH  
• Damage free monolayer doping  
• Plasma doping  
• Anneal: ms (flash, laser, spike) |
| Resistor  | ![Resistor Diagram] | • Linearity  
• Heat Dissipation  
• FINFET, MG | • Thin metal  
• Materials screening for TCR  
• ↓ Parasitic R | • Tune $R_{co}$ NiSi-Si  
• O, Si, N implant  
• TaN optimization (C, N, O) for TCR  
• W system  
• I-V measurements |
| Inductor  | ![Inductor Diagram] | • Linearity  
• Area Scaling (induct/µm²)  
• Capacitive coupling | • 3-D/ serpentine coils  
• Remove Si between coils  
• ↓ Parasitic R | • 3-D test structure  
• Series Resistance  
• High freq capability to 40GHz |
| Capacitor | ![Capacitor Diagram] | • Linearity  
• Area scaling (cap/µm²) | • SEMATECH solution to 2013  
• Higher k | • VCC<<100  
• Vg<10⁻⁷ A/cm²  
• Cap den=7fF/µm²  
• Work with tool supplier  
• Etch / etch stop development.  
• Conformal process |

**SEMATECH Contribution**

- Dipole tuning SBH
- N Implant tuning SBH
- Damage free monolayer doping
- Plasma doping
- Anneal: ms (flash, laser, spike)
- Tune $R_{co}$ NiSi-Si
- O, Si, N implant
- TaN optimization (C, N, O) for TCR
- W system
- I-V measurements
- 3-D test structure
- Series Resistance
- High freq capability to 40GHz
- VCC<<100
- Vg<10⁻⁷ A/cm²
- Cap den=7fF/µm²
- Work with tool supplier
- Etch / etch stop development.
- Conformal process
2009 ITRS: Overview of scaling trends

Moore’s Law & More

Functional Diversification (More than Moore)

- Analog/RF
- HV Power
- Passives
- Sensors
- Actuators
- Biochips

Continuing SoC and SiP: Higher Value Systems

Beyond CMOS

Traditional Models

Scaling (More Moore)

[Geometrical & Equivalent scaling]

Baseline CMOS: CPU, Memory, Logic

- 130nm
- 90nm
- 65nm
- 45nm
- 32nm
- 22nm
- ...V

Information Processing

Digital content

System-on-chip (SoC)

Non-digital content

System-in-package (SiP)

Interacting with people and environment

SIP “White Paper”
A&P ITWG
www.itrs.net/papers.html
Logic and memory roadmap
Technologies converge for higher value solutions

Advanced Materials
- Bulk/SOI Si
- HfOₓ
- Si
- High-μ Fin/NW
- Metal
- High-k
- InGaAs

Advanced Structures
- High μ Fin/NW
- Si Nanowire
- SiGe
- Si
- High mobility Fins/Nanowires

Beyond CMOS Materials/Structures
- SEMATECH
- ReRAM
- TFET
- NEMS
- Graphene

Logic
- Gate stack
- Channels, contacts, USJ
- 20 nm
- {100}
- SiGe

Memory
- CT Flash
- ReRAM
- 1T DRAM
- <20nm ReRAM
- ReRAM/Nanowire 3DArray

2009
2011
2013
2015
2017
2019

High mobility
Fins/Nanowires
Summary

- More Moore or More than Moore is **NOT** the question
  - Sense, compute, store, transmit: Integrated functionality
- Convergence of technologies is the future
  - System level power reduction with performance gain is key
- Functional diversity vs device density
  - Focus of miniaturization shifts to adding diverse components
  - CMOS+: Hybrid integration of beyond-CMOS with CMOS
  - Challenge: How can we fabricate them and make them work seamlessly
- Fundamental shift in memory to non-charge-based memory
  - Embedded memory for level 3/4 cache
  - Reconfigurable memory-logic devices in the horizon
- 3D Interconnects is a game changer
- Process-Integration-Design co-optimization is a must
Accelerating the next technology revolution