Asynchronously Controlled Frequency Locked Loop

async techniques in a sync system

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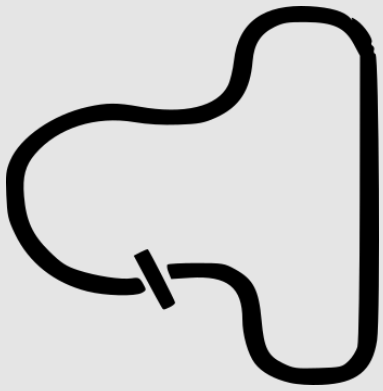
The Big Picture

Circuit

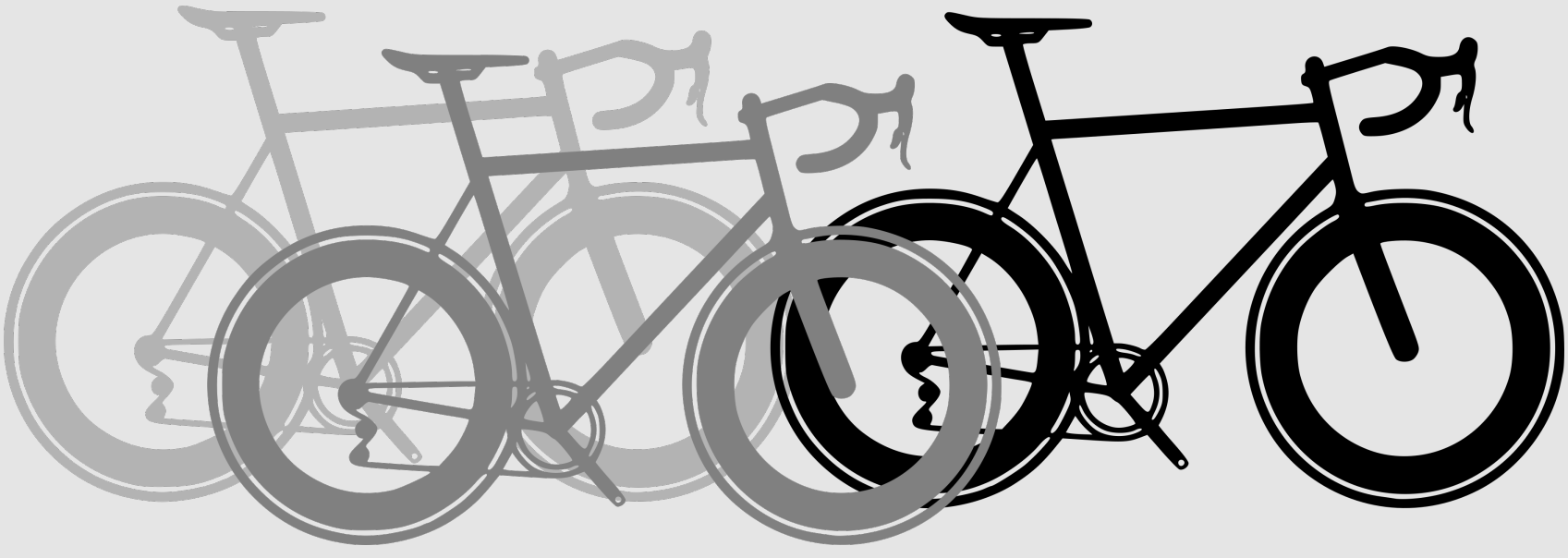


Rate

Optimize performance

The Big Picture

Matching speeds



Applications and prior

Apps

- PLL : sep. phase and freq loops, or coarseness
- Dist power grid sync : small freq. variations
- Frequency synthesis : lower loop order
- Capacitance measurement : measure osc. freq

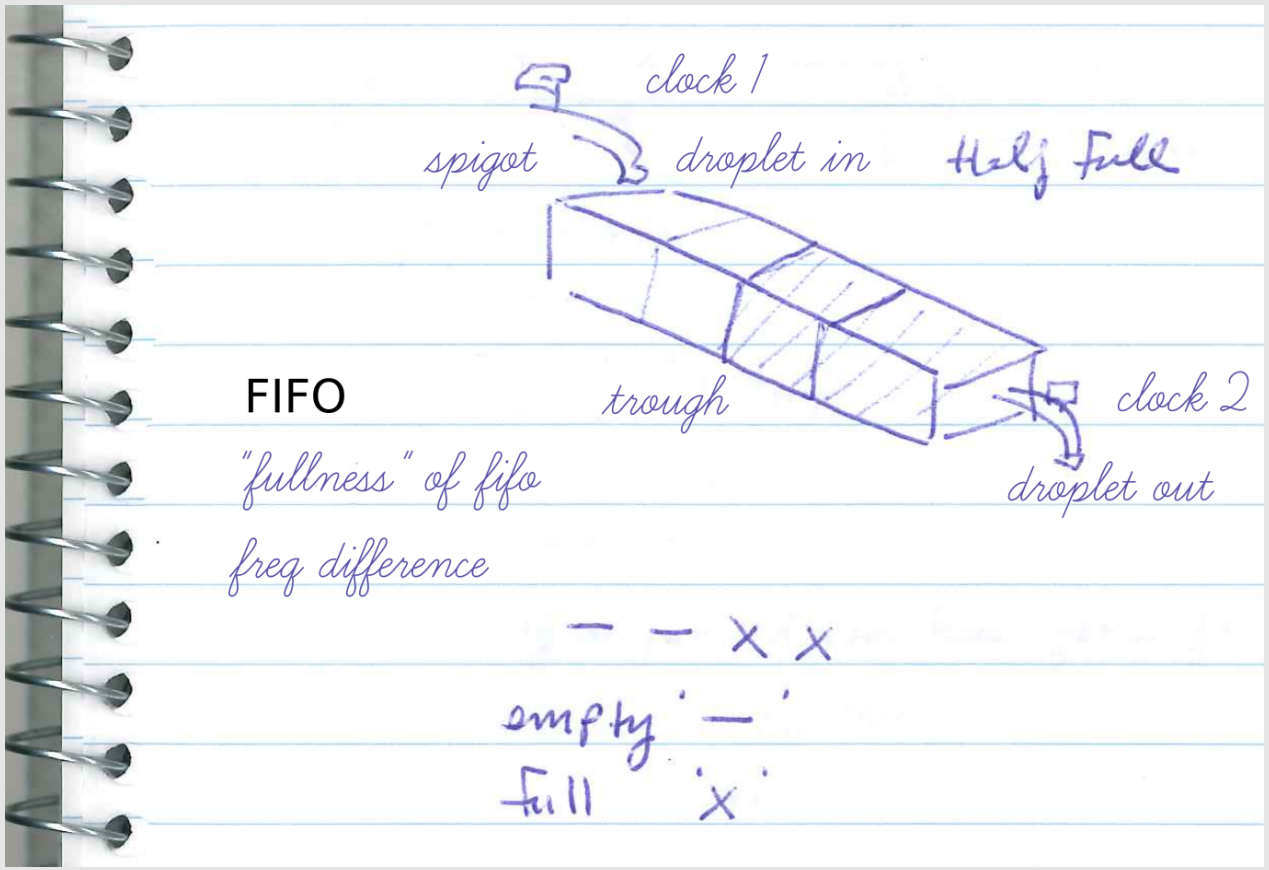
Applications and prior

Prior

- Counters
- Sigma-delta noise shaping modulators
- Frequency-to-voltage conversion
- Second-order integrators

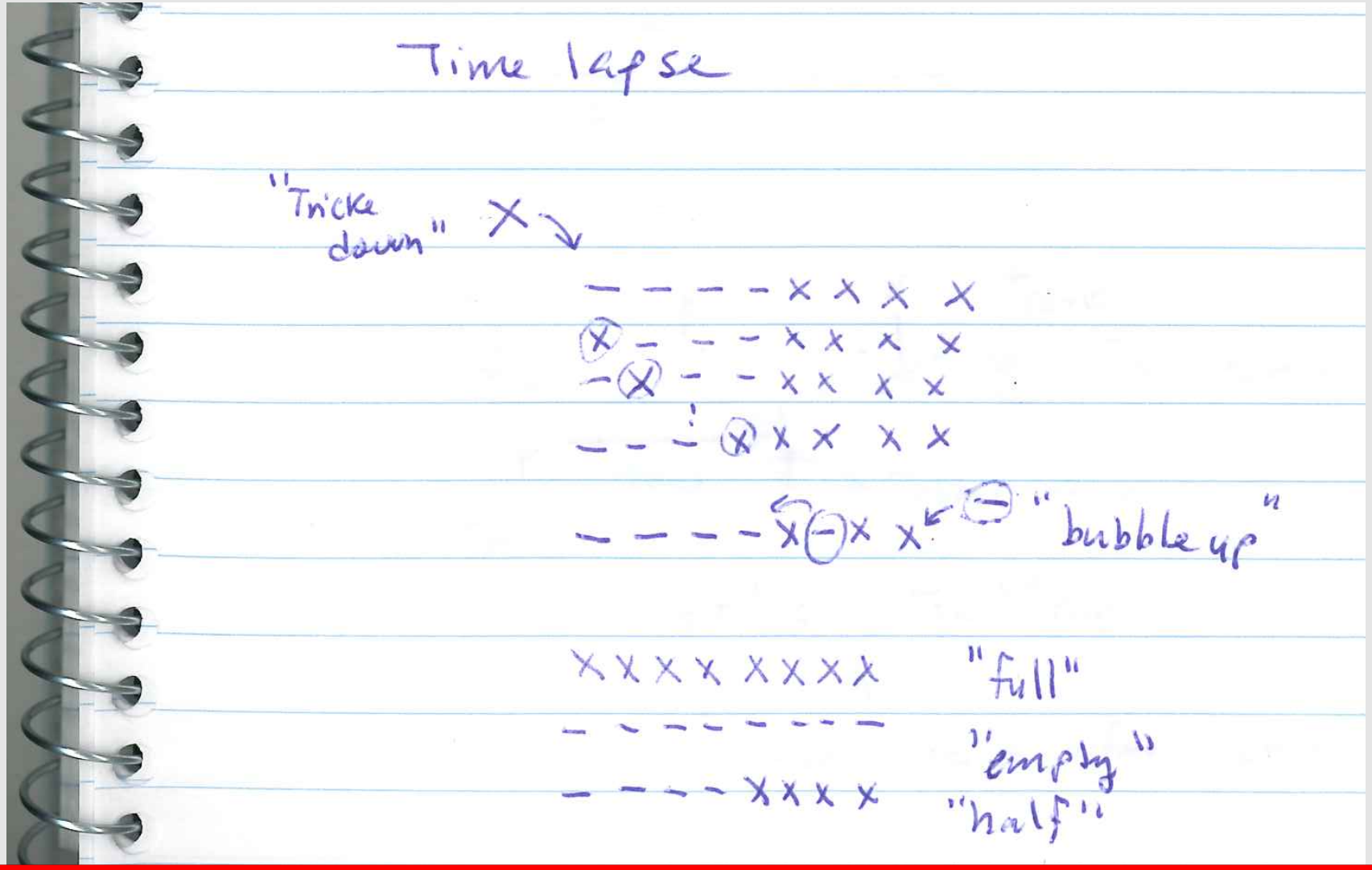
Asynchronous FIFO for frequency detection

Spigots in Minecraft



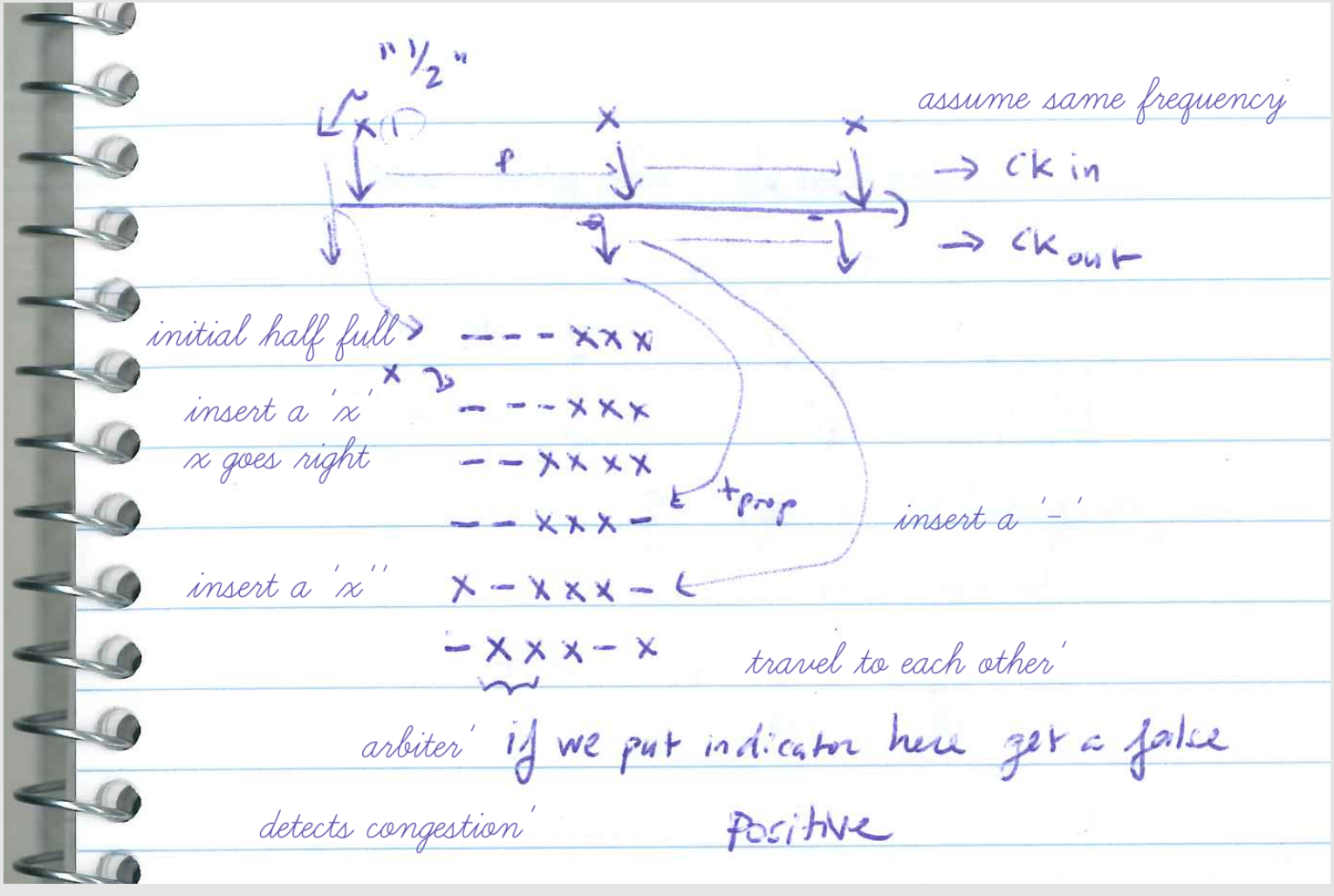
Symbology

Tic tac toe



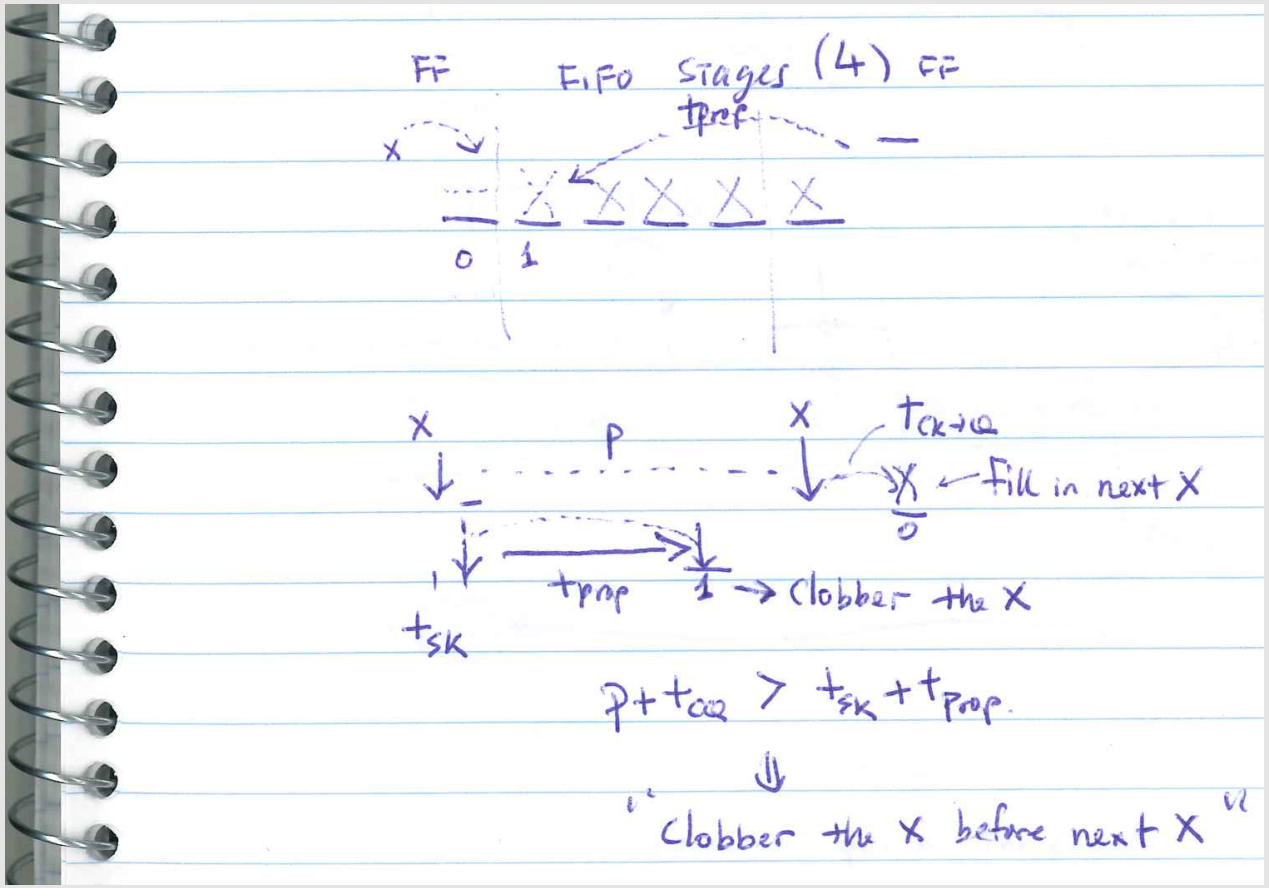
False positive

I am a Cylon



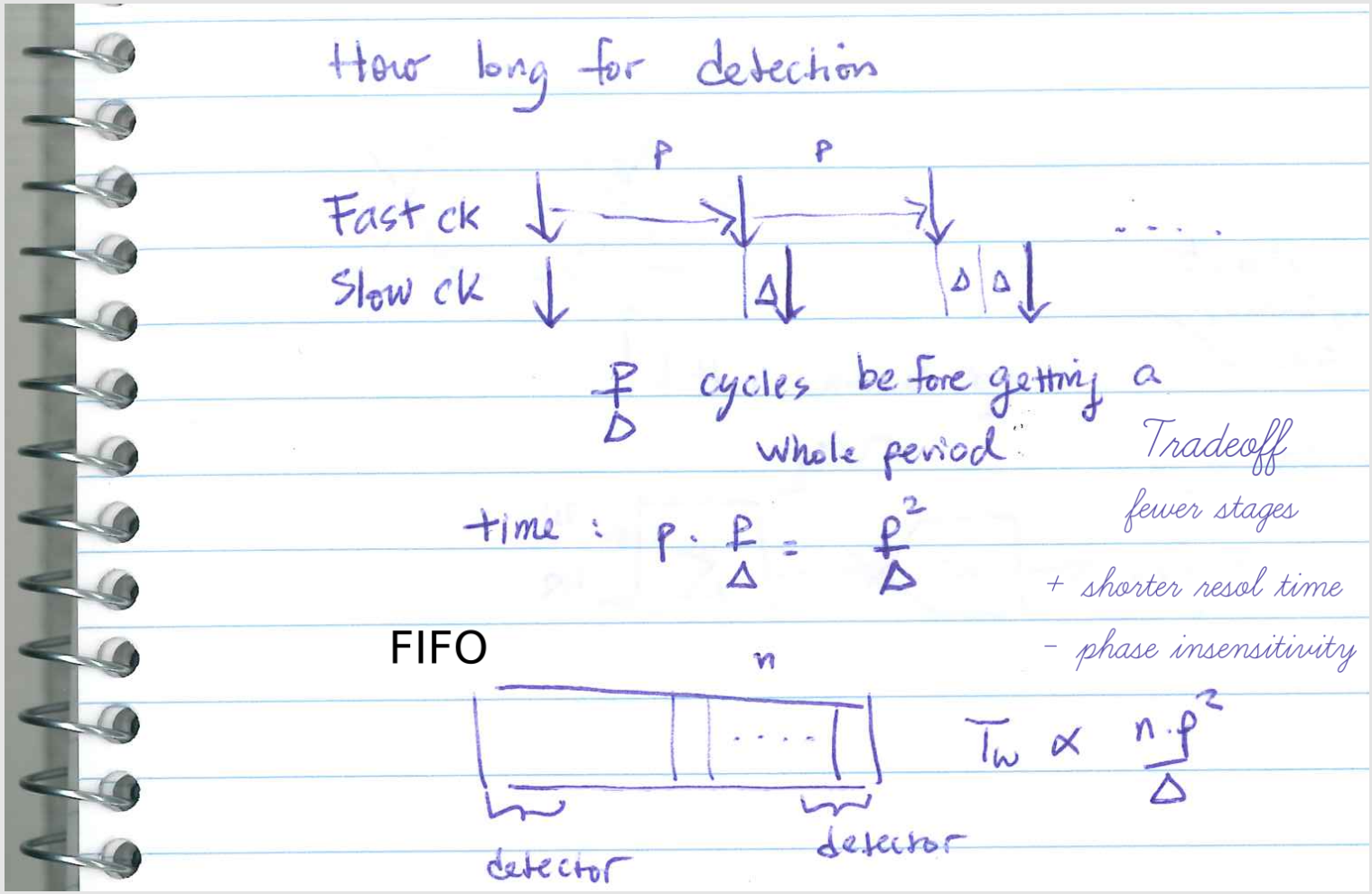
Clobber

Wack the mole



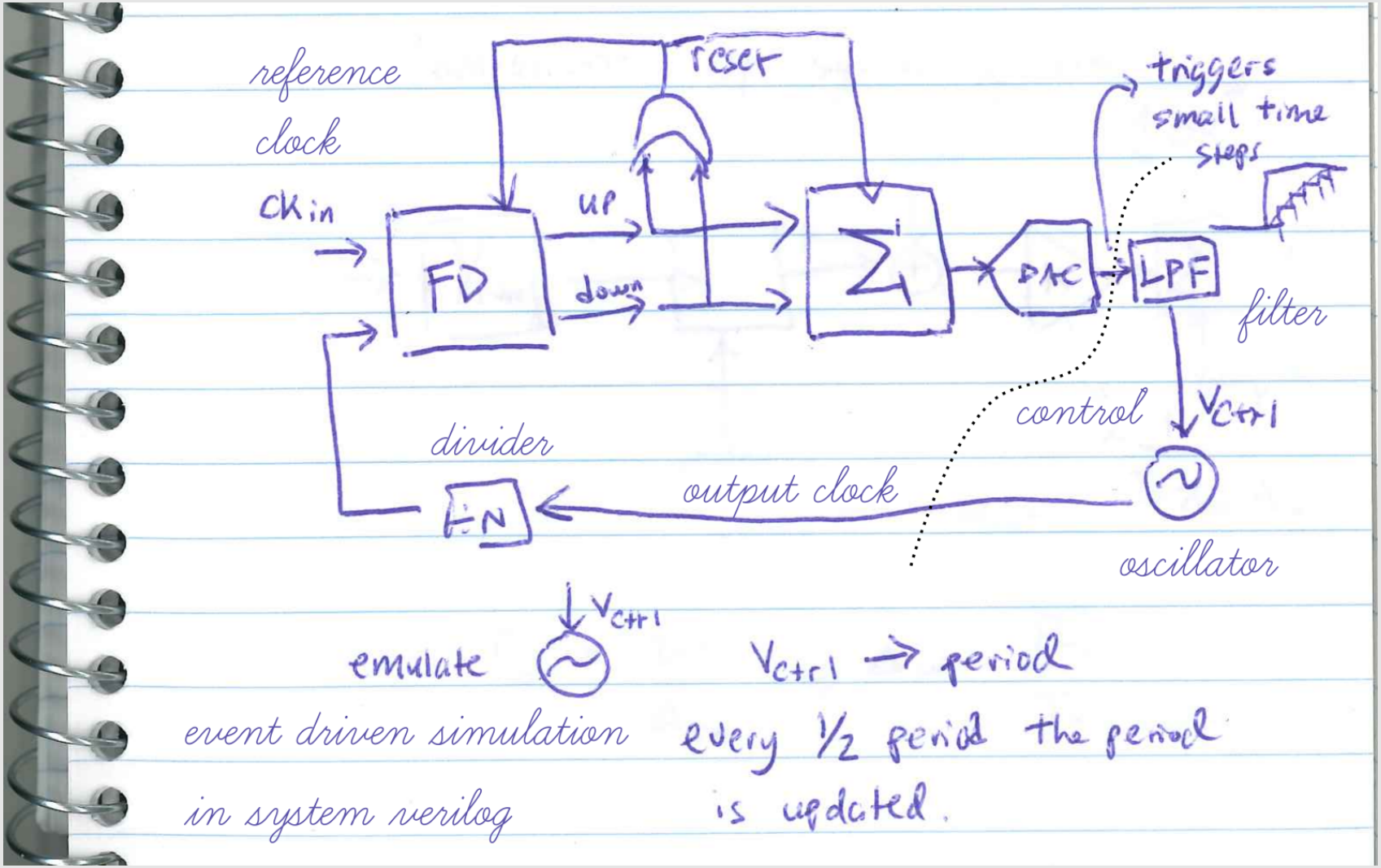
How long before an update

Check, please



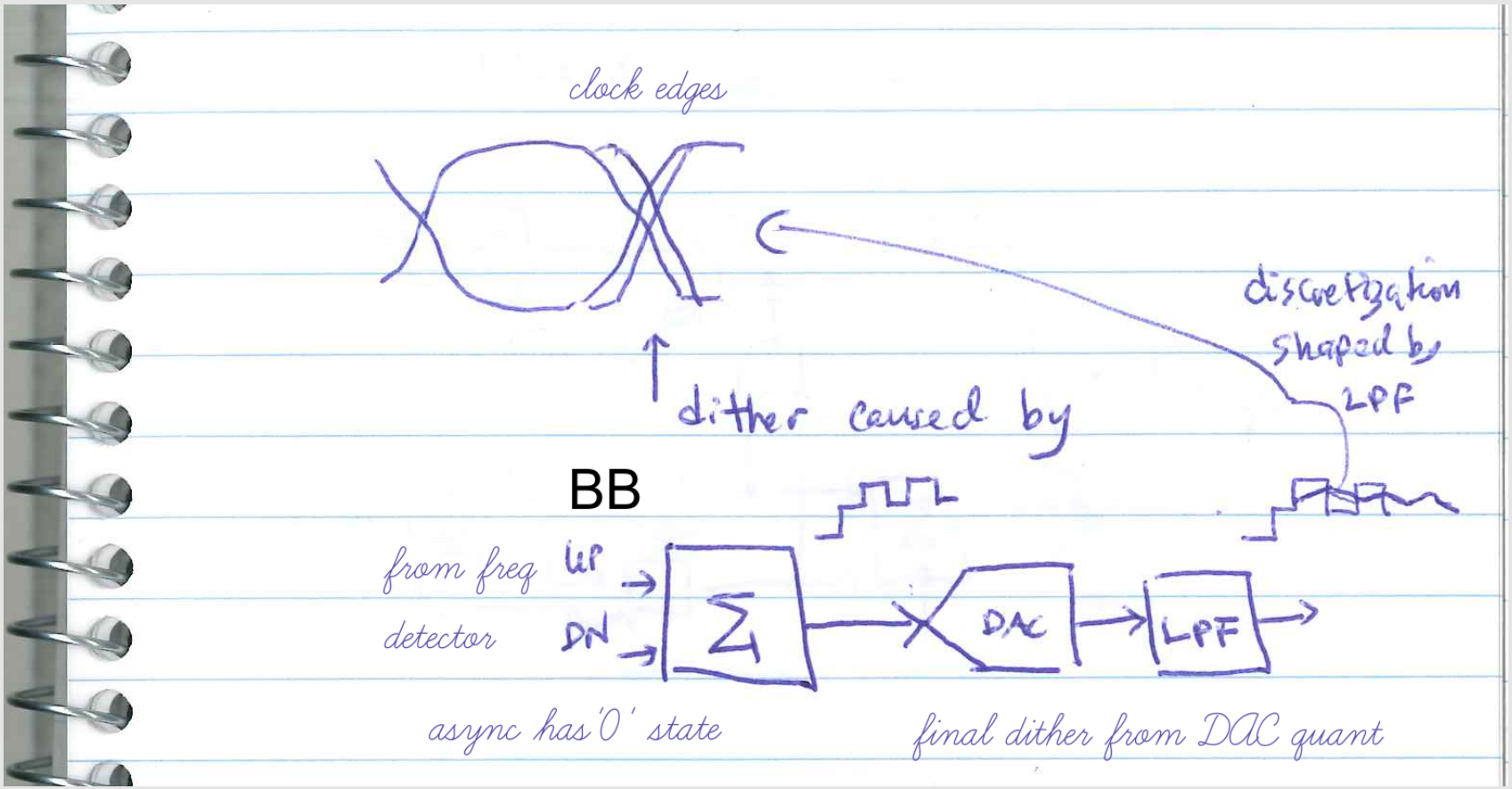
FLL with the frequency detector

In a system



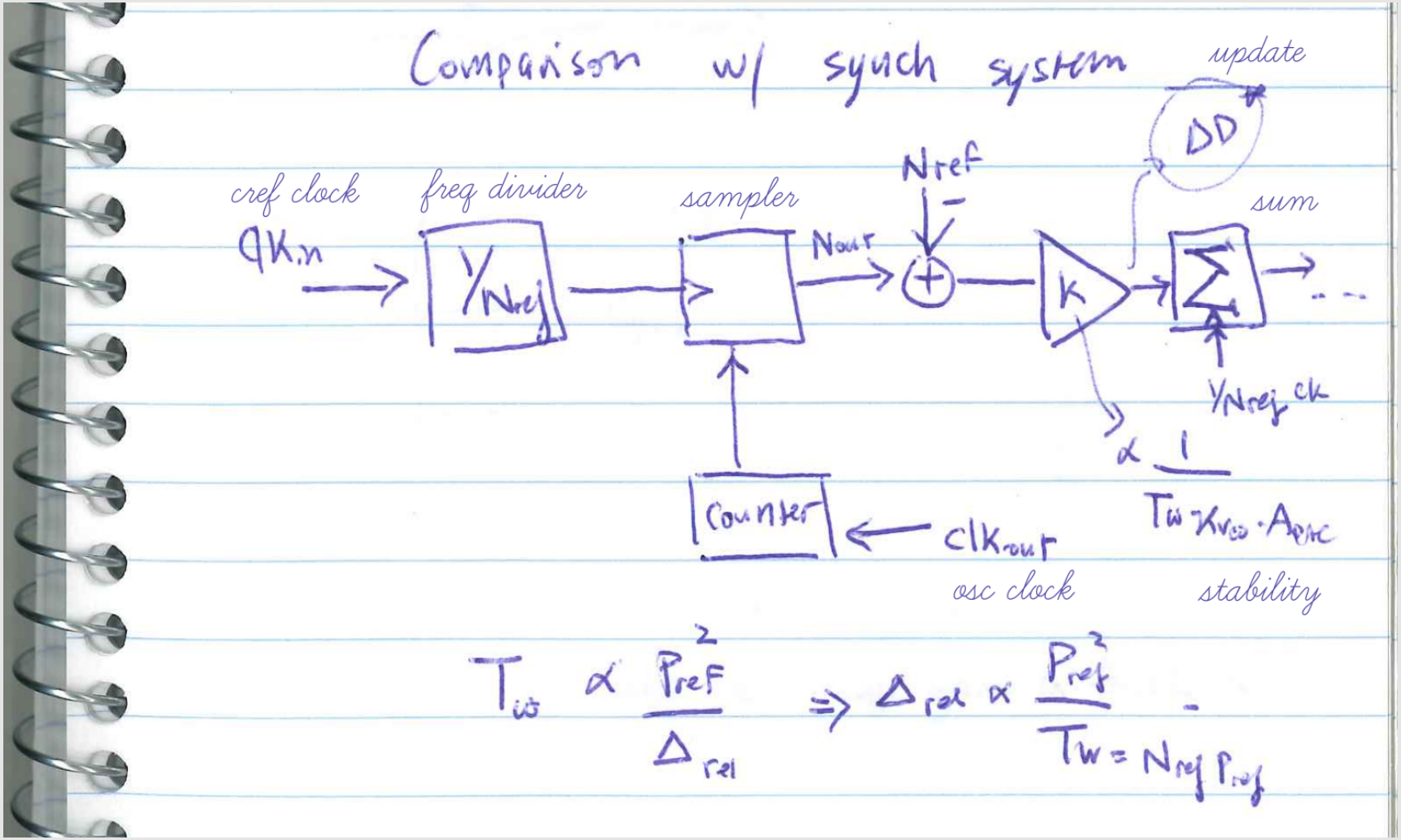
Dither

What is that fuzz



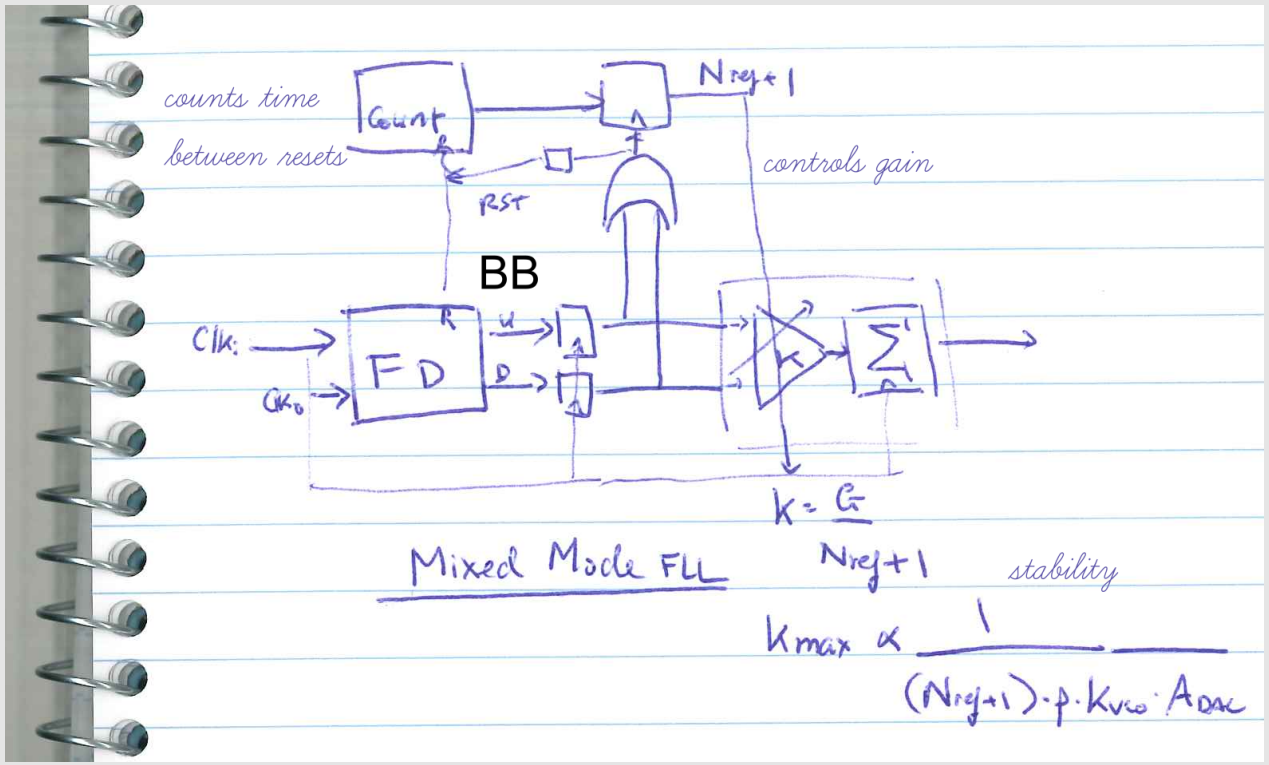
Synchronous counting

By the clock



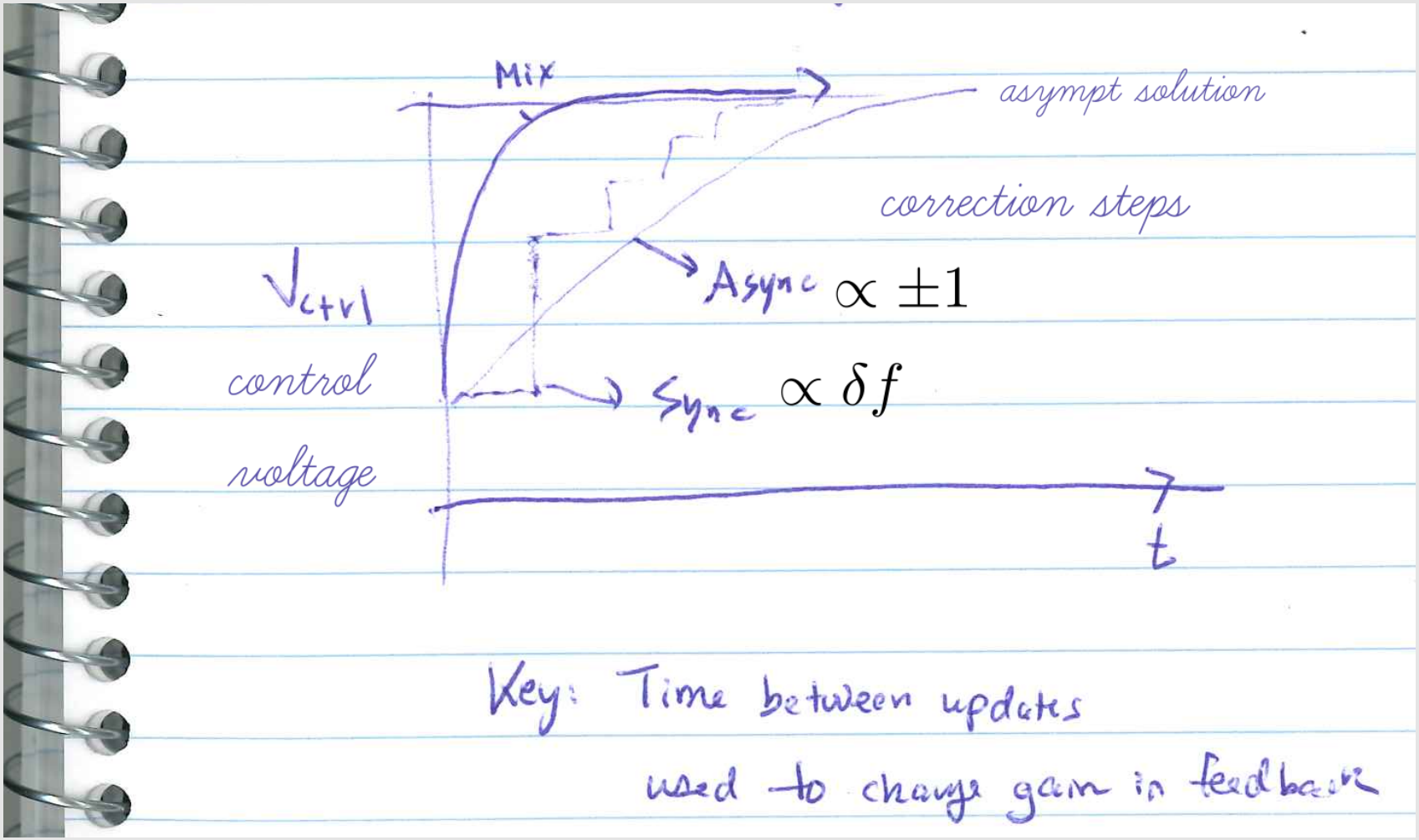
Mixed Mode FLL

Lock faster



Time traces for oscillator control voltage

Show and tell



Ending

There is no place like home

- Pro: simple design FLL, resolution not set by large number of bits, fixed "space" requirement
- Pro: not sensitive to phase offset between the two signals
- Pro: static jitter set by DAC quantization error
- Pro: fast locking via gear shifting, done in an asynchronous manner, goes with the flow
- Con: adoption of non time-synchronous solution

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Questions ?

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