Ring Oscillator Clocks and Margins

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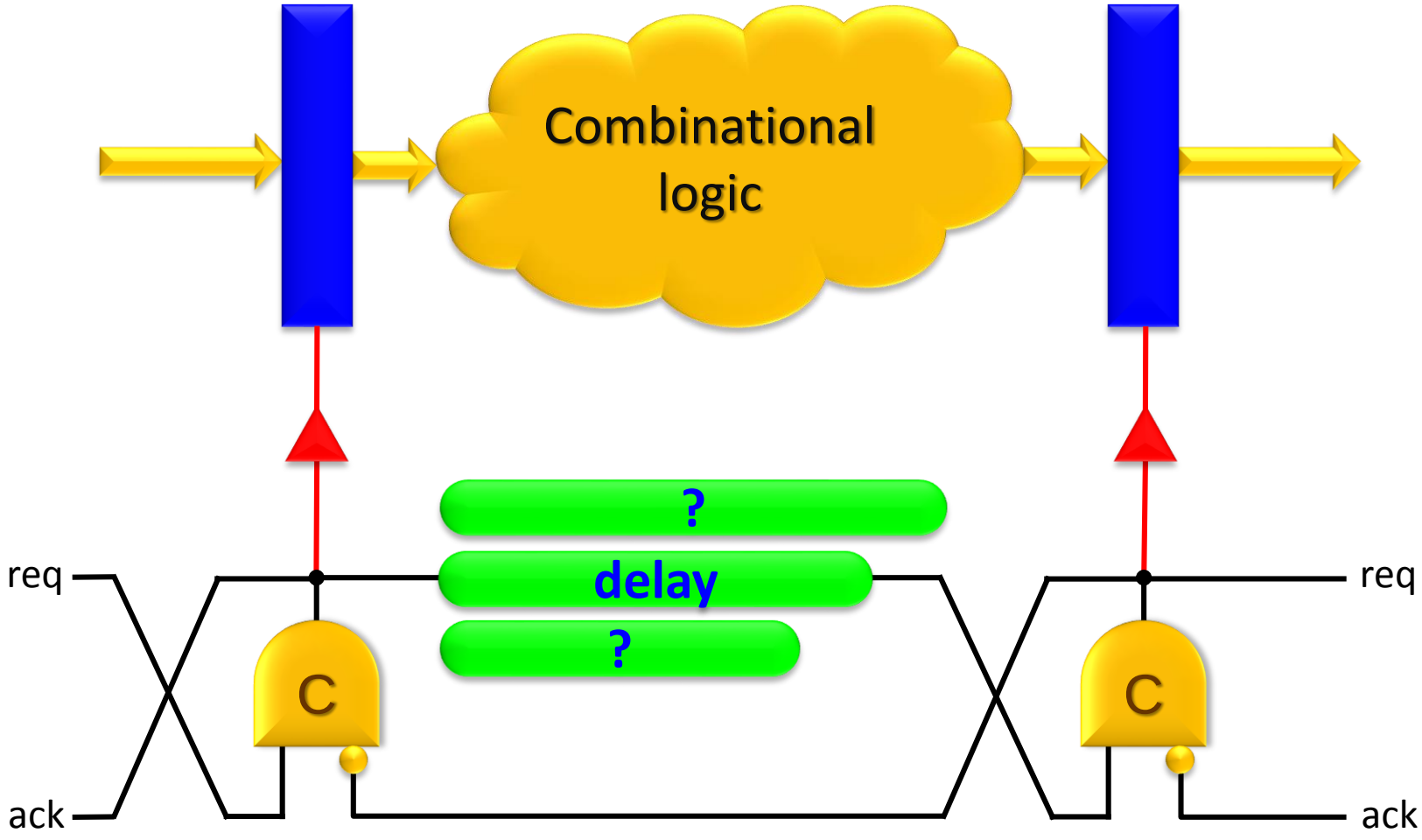
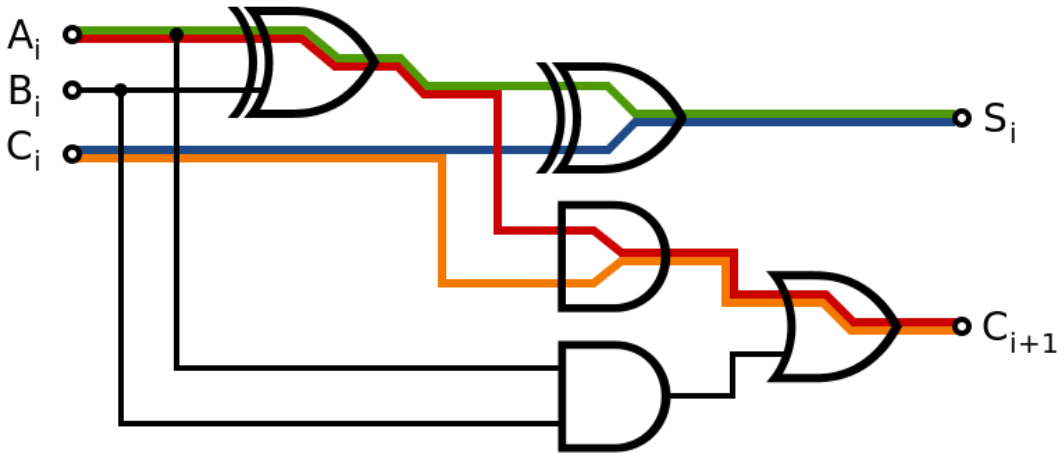
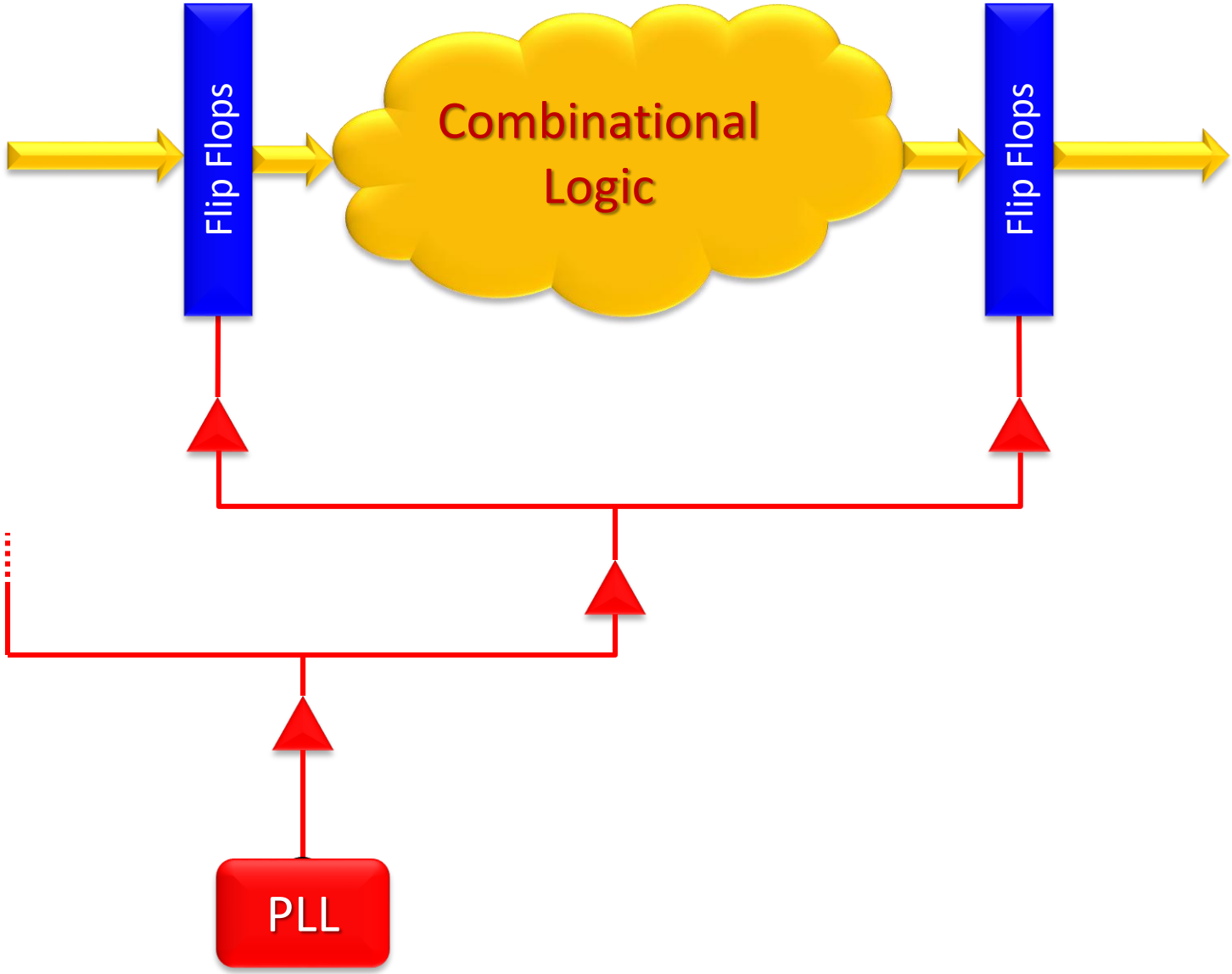
Matched delay: is it long enough?



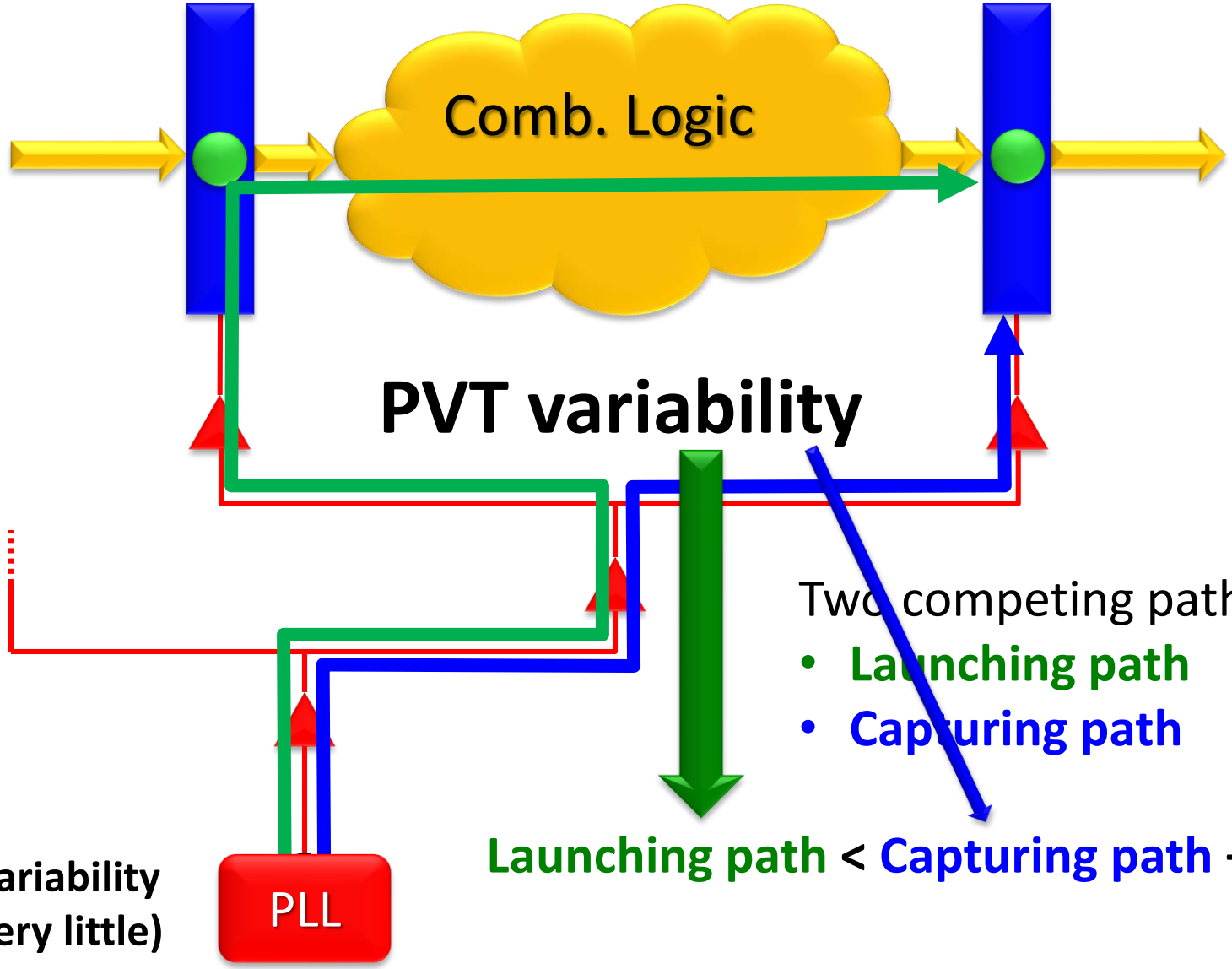
Static Timing Analysis



Static Timing Analysis



Static Timing Analysis: setup constraint



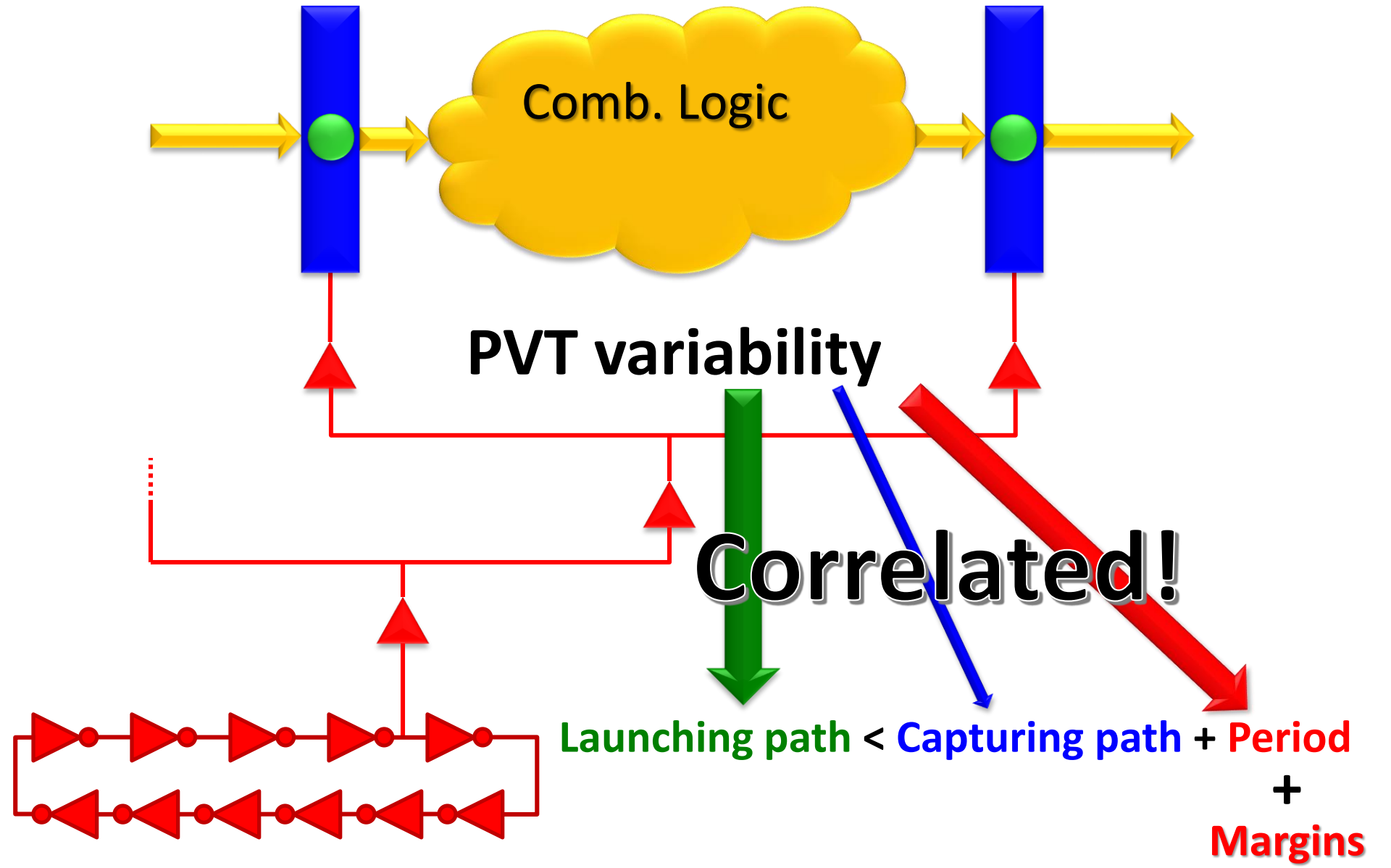
No variability
(or very little)

Two competing paths:

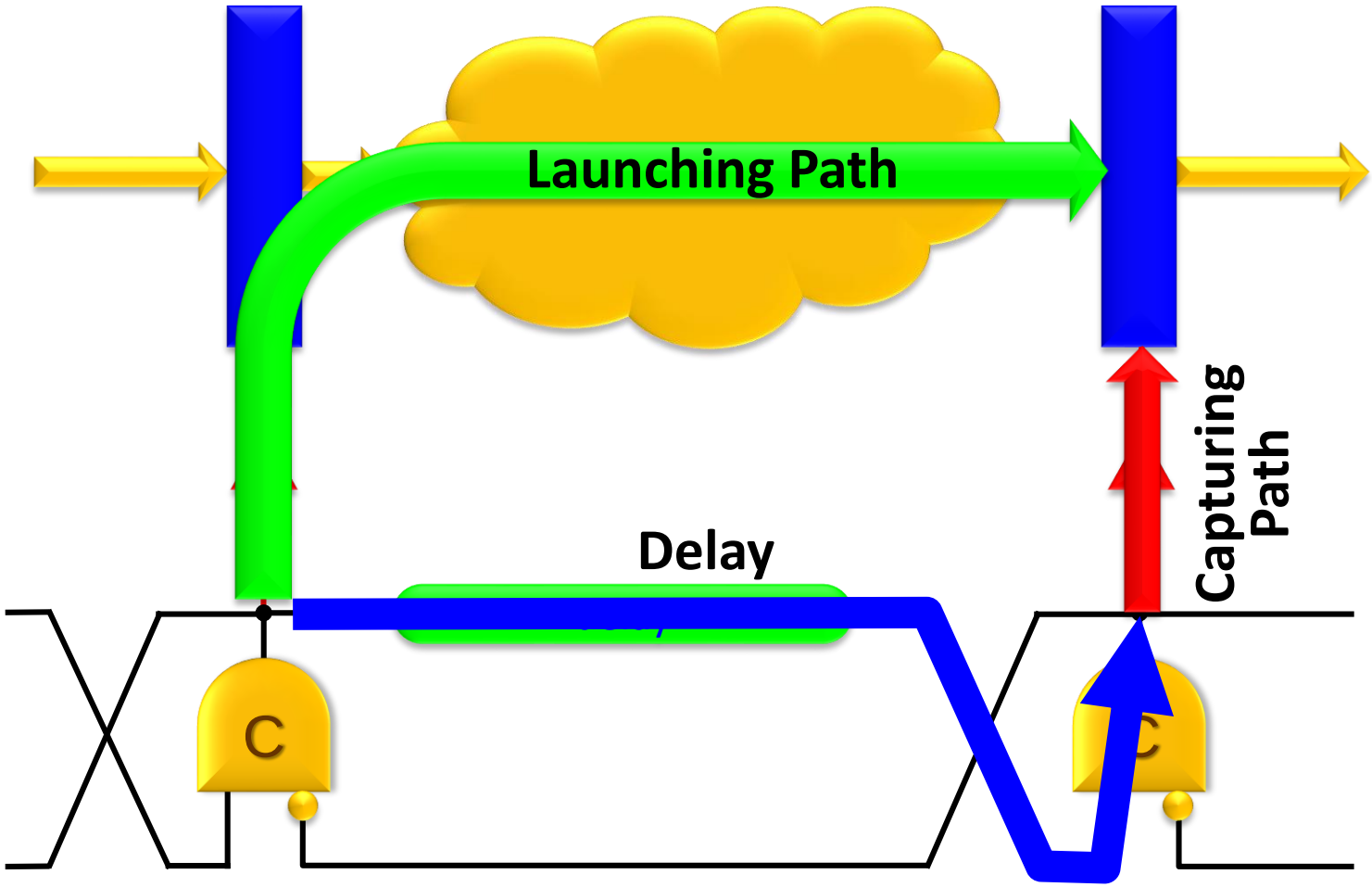
- Launching path
- Capturing path

Launching path < Capturing path + Period
+
Margins

Ring Oscillator

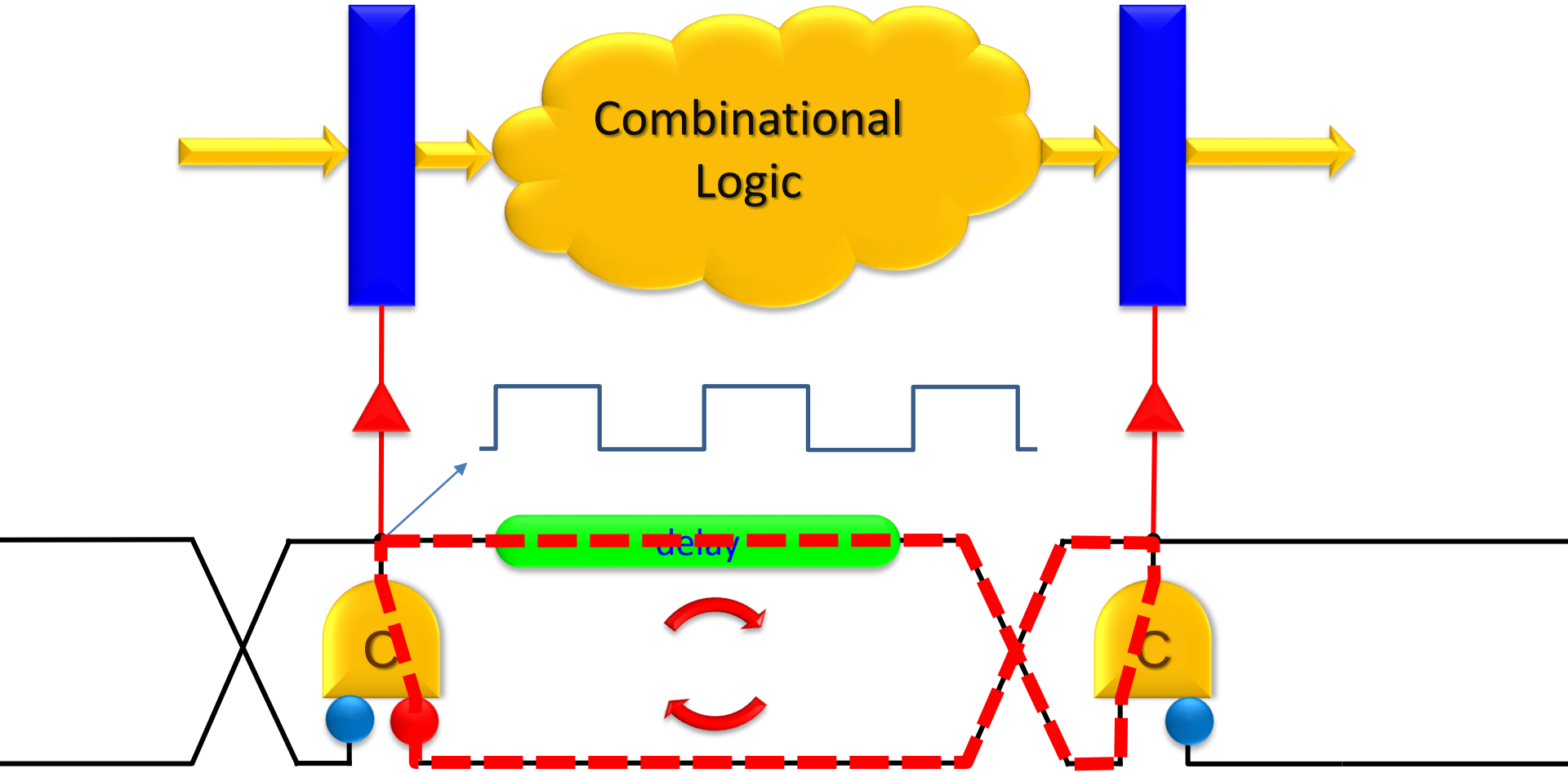


Matched delays: setup constraint



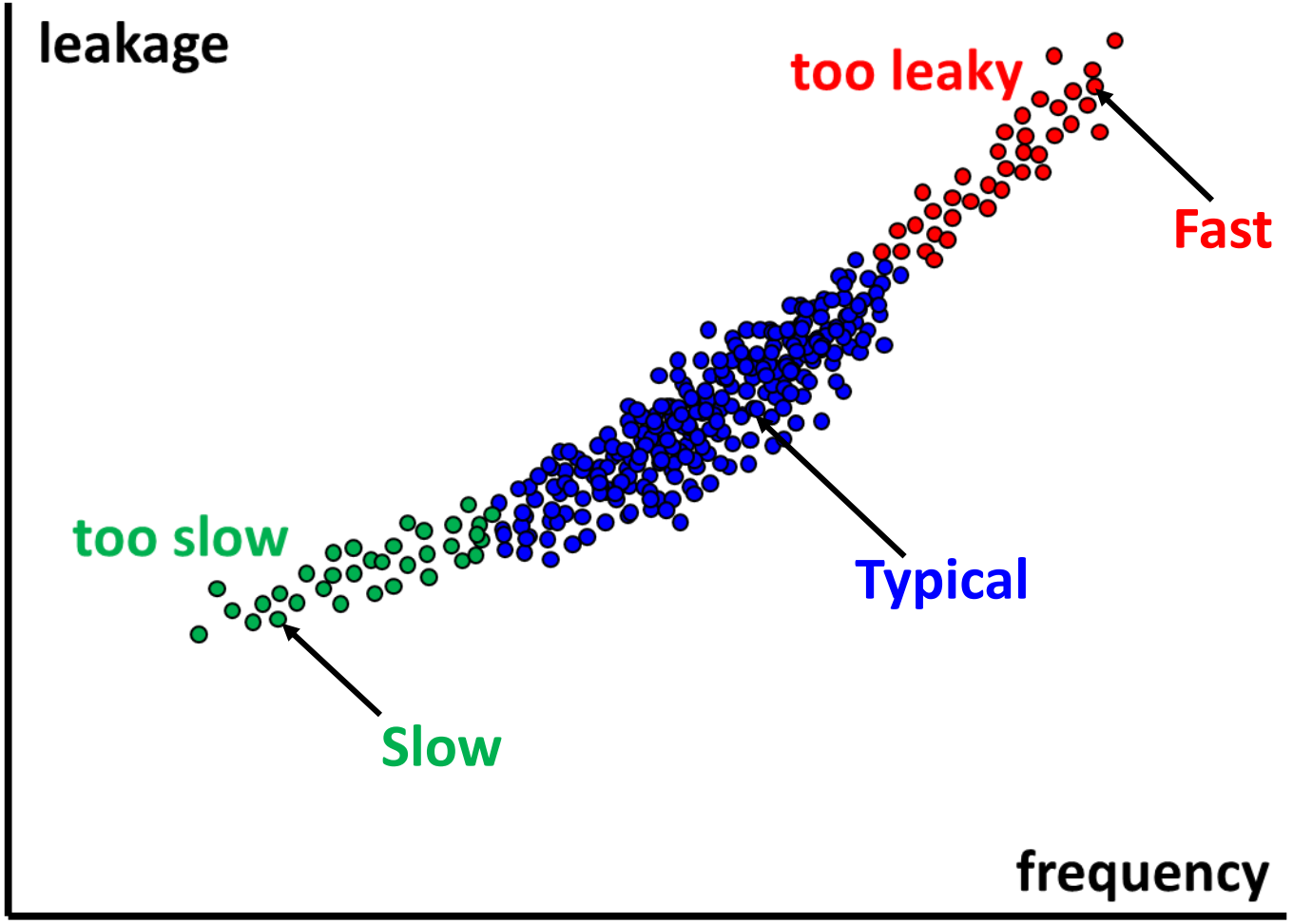
Launching path < Capturing path + Delay ⟸ (Margins?)

Handshaking Ring Oscillators

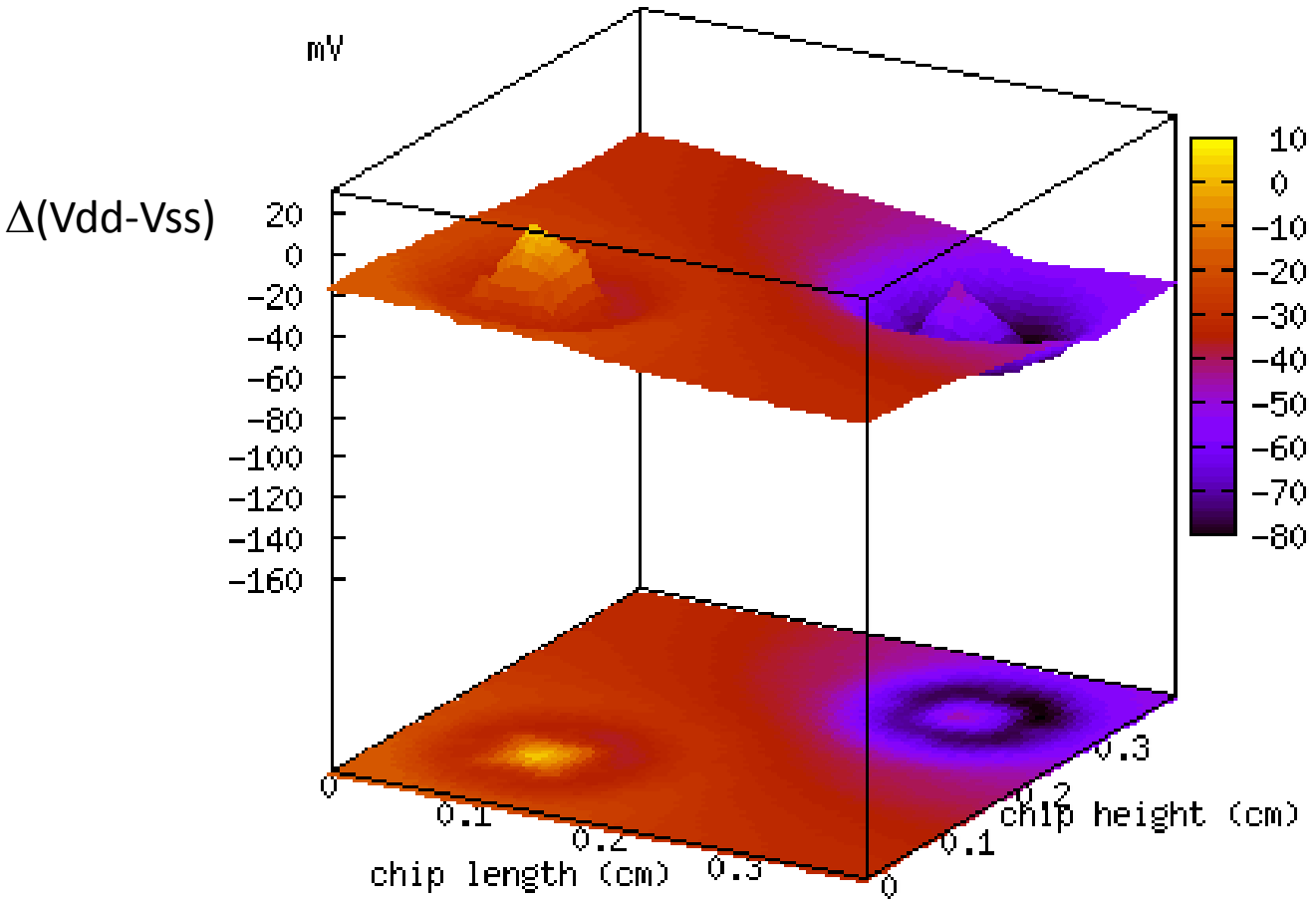


Understanding variability

Process variability

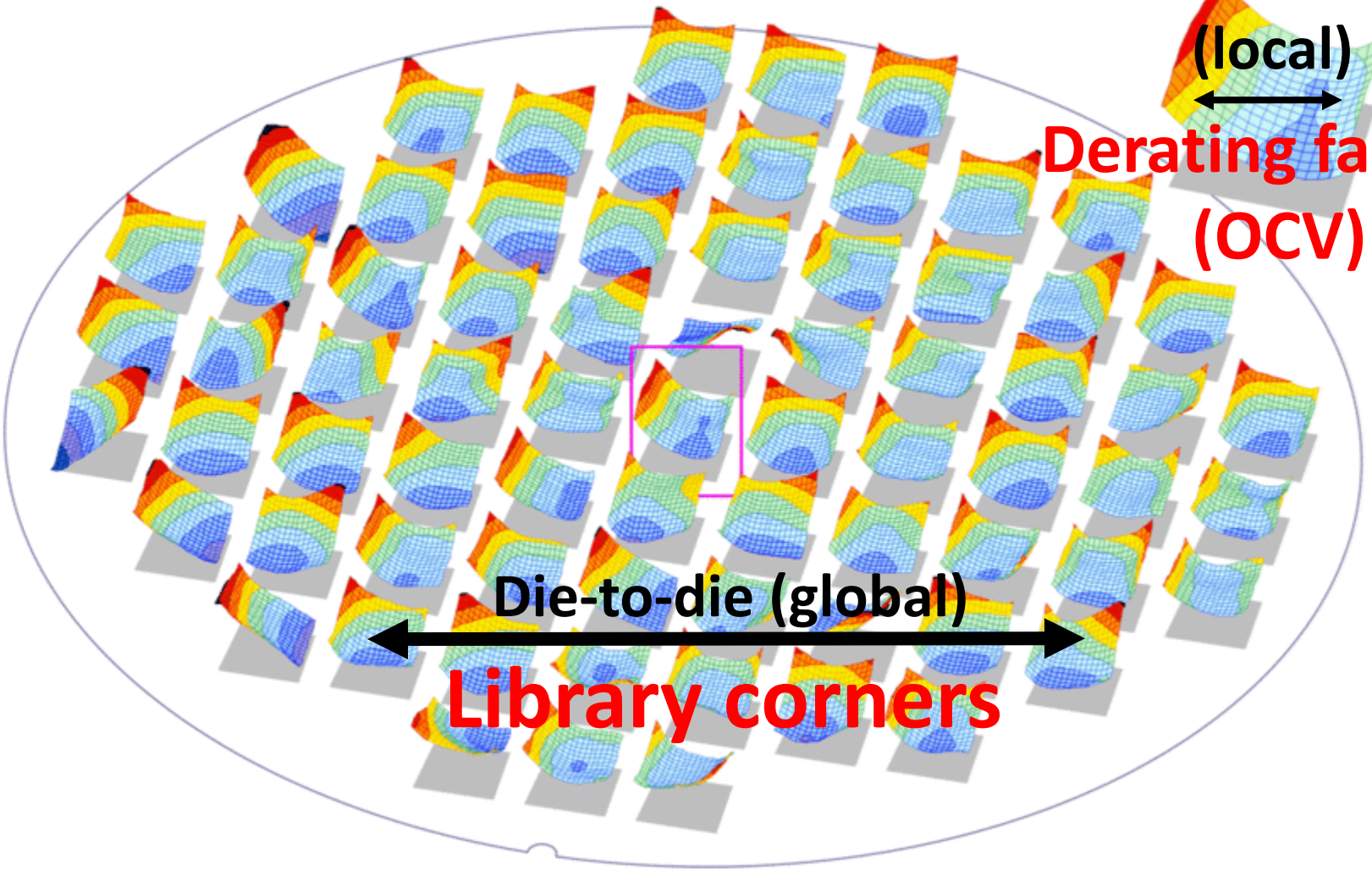


Dynamic variability



Raj Nair (Anasim Corp.),
IC floorplanning and Power Integrity, SOCcentral, Aug 2, 2010.
http://www.soccentral.com/results.asp?entryID=31901.

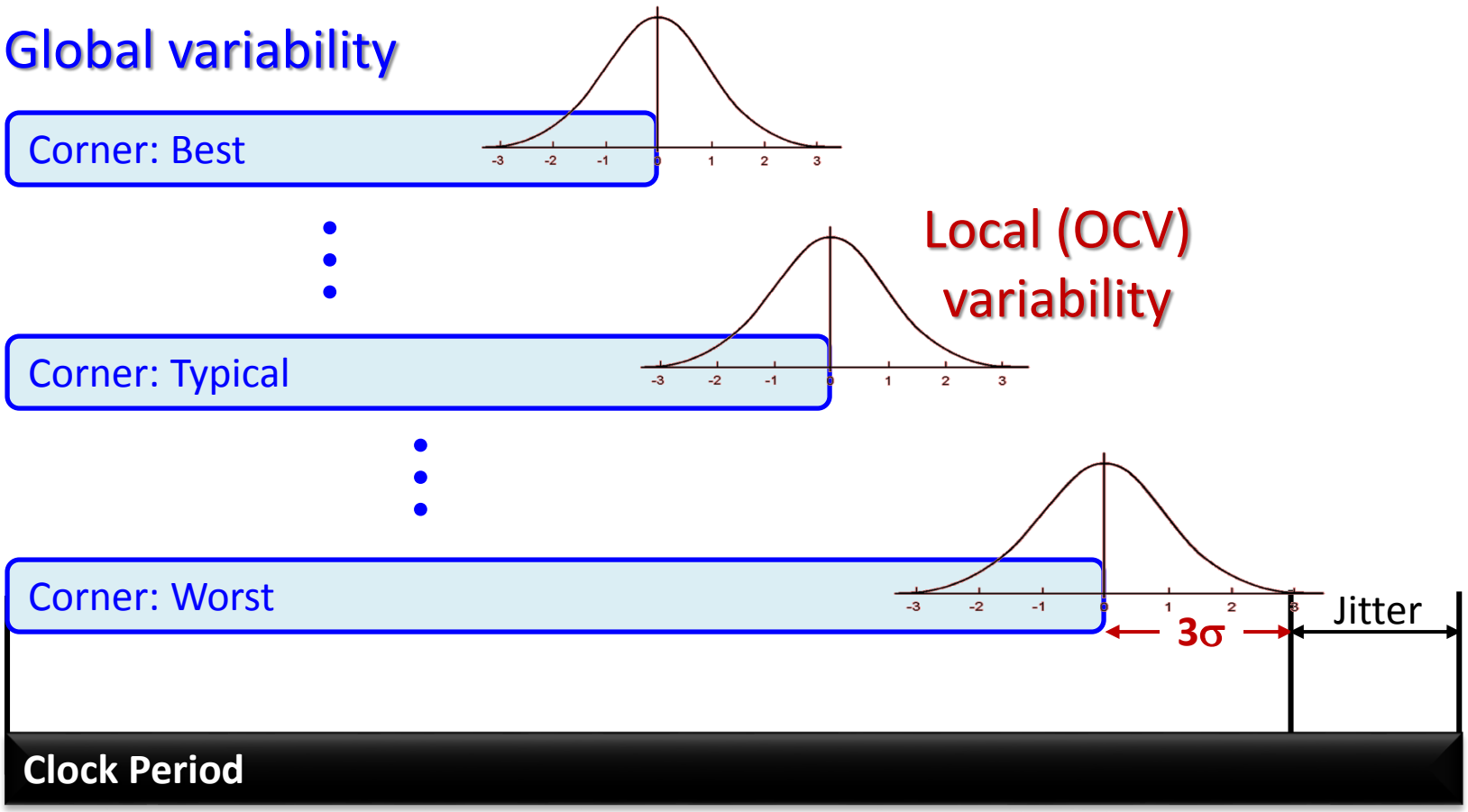
Variability during STA



Source: H. Masuda et al. (ICICC 2005)

Timing sign-off

Timing sign-off

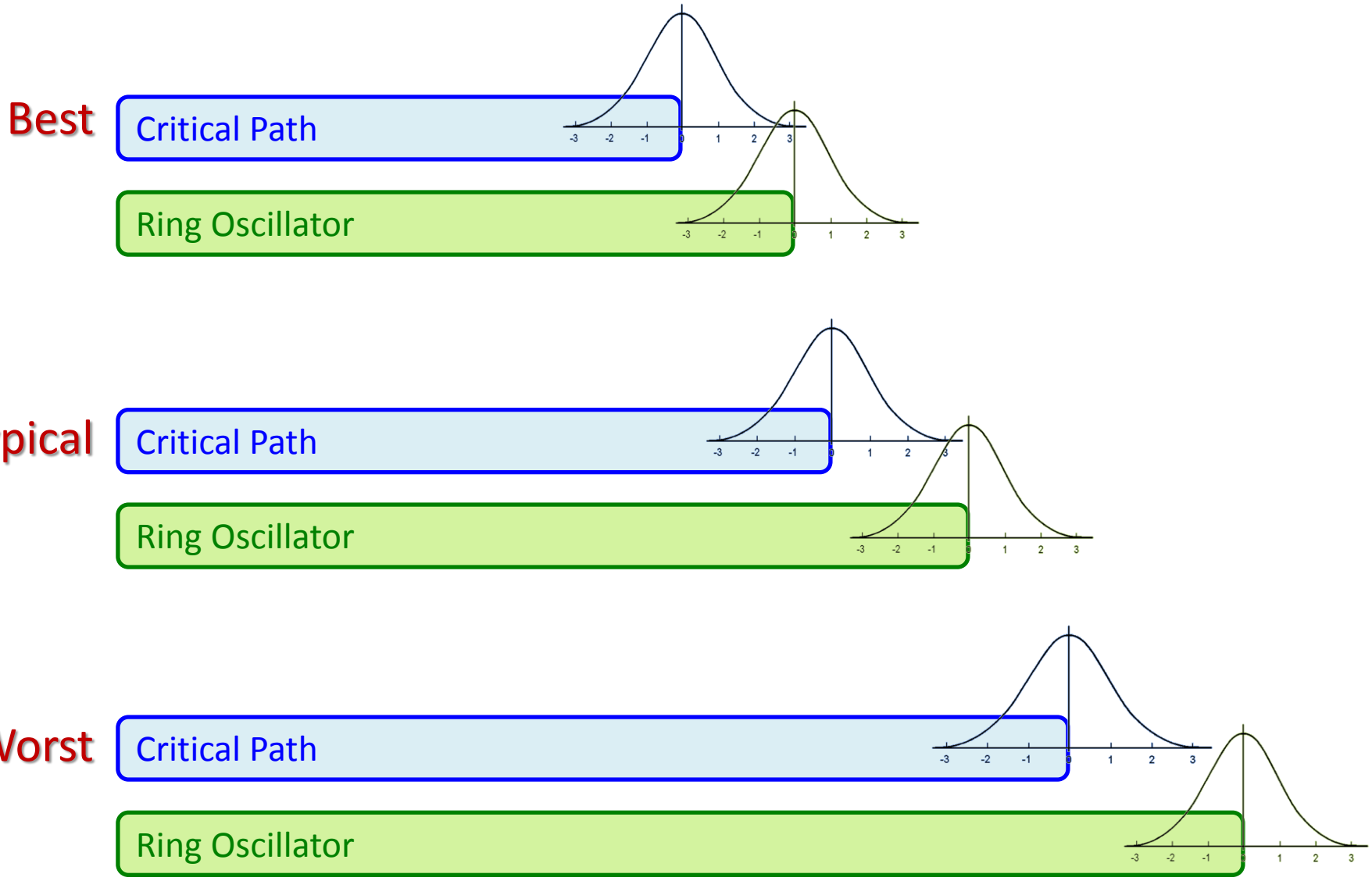


$(1+\delta) \cdot \text{PathDelay} < \textit{Period} - \text{Jitter}$

OCV derating factor

typical $\delta \approx$ 0.05 … 0.15

Timing sign-off with ROs



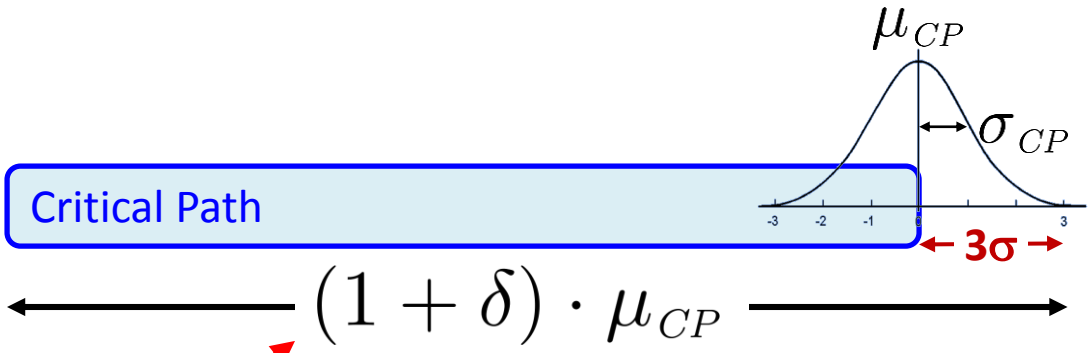
Timing sign-off with ROs

- Goal: doing *classical timing sign-off* using
  - conventional STA tools
  - designer's library corners and OCV derating factors

- In the paper you will find
  - A more sophisticated statistical delay model (1^{st}-order Taylor expansions for variability)

- This presentation:
  - A simpler and complementary variability model
  - Similar conclusions as the ones in the paper

Timing sign-off delay model

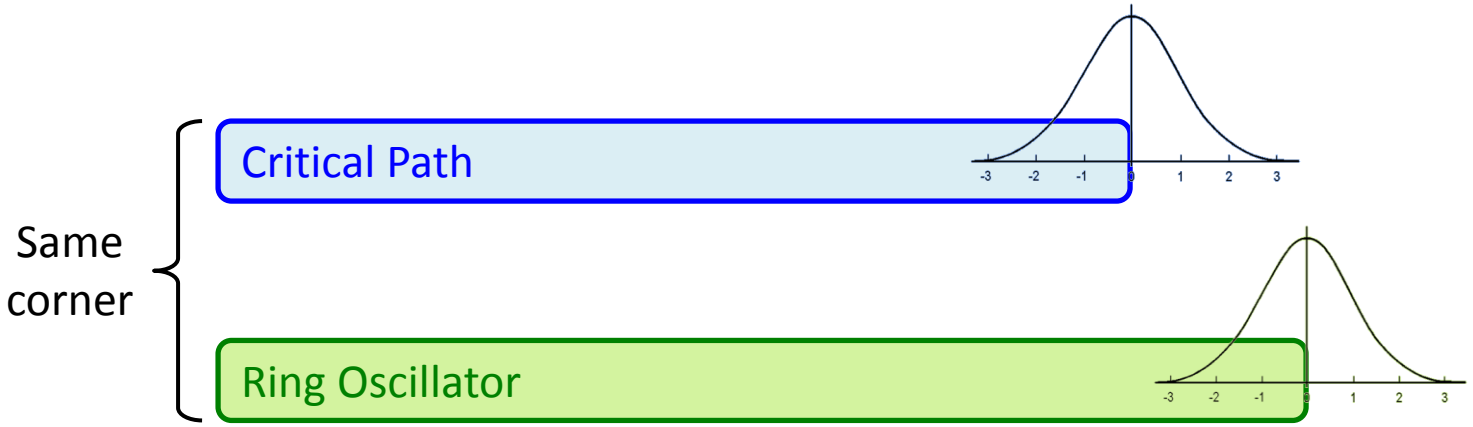


$$D_{CP} \sim \mathcal{N}(\mu_{CP}, \sigma_{CP}^2)$$

$$(1+\delta)\cdot\mu_{CP} = \mu_{CP} + k\cdot\sigma_{CP}$$

$$\delta = \frac{k\cdot\sigma_{CP}}{\mu_{CP}}$$

Timing sign-off delay model with ROs



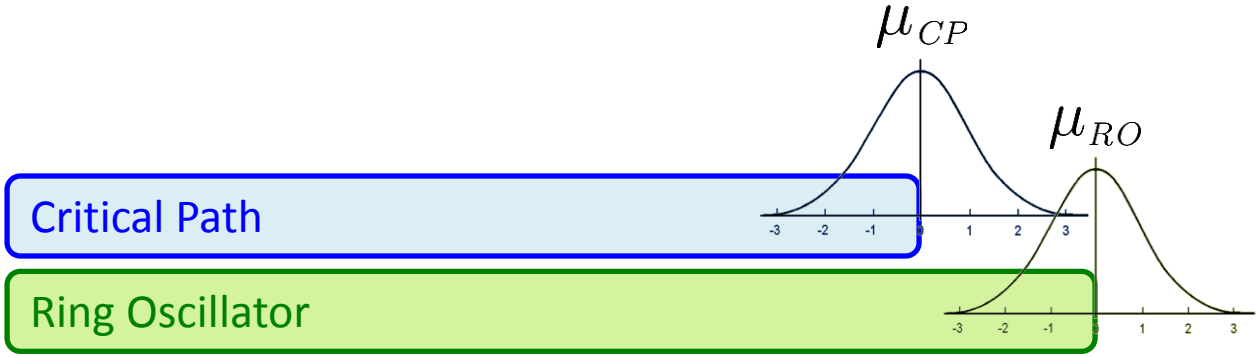
$$D_{CP} \sim \mathcal{N}(\mu_{CP}, \sigma_{CP}^2)$$

$$D_{RO} \sim \mathcal{N}(\mu_{RO}, \sigma_{RO}^2)$$

$$D_{RO} - D_{CP} \sim \mathcal{N}(\mu_{RO} - \mu_{CP}, \sigma_{RO}^2 + \sigma_{CP}^2)$$

$$\underbrace{\mu_{RO} - \mu_{CP}}_{\mu} - k \underbrace{\sqrt{\sigma_{RO}^2 + \sigma_{CP}^2}}_{\sigma} > 0$$

Timing sign-off model with ROs



Assumption: similar index of dispersion (variance-to-mean ratio)

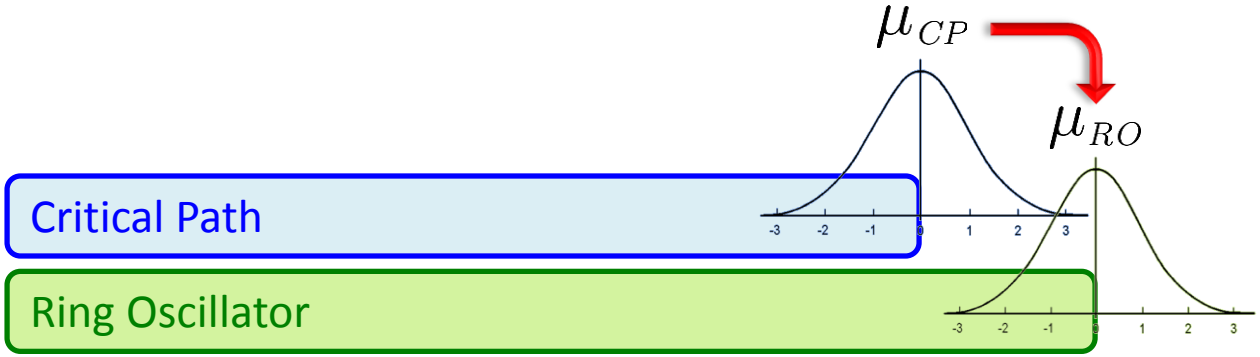
$$\frac{\sigma_{RO}^2}{\mu_{RO}} \simeq \frac{\sigma_{CP}^2}{\mu_{CP}}$$

new derating factor

$$\mu_{RO} > \left(1 + \frac{\delta\sqrt{8+\delta^2}+\delta^2}{2}\right)\mu_{CP}$$

$$\underbrace{\mu_{RO} - \mu_{CP}}_{\mu} - k\underbrace{\sqrt{\sigma_{RO}^2 + \sigma_{CP}^2}}_{\sigma} > 0$$

Timing sign-off model with ROs



Assumption: similar index of dispersion (variance-to-mean ratio)

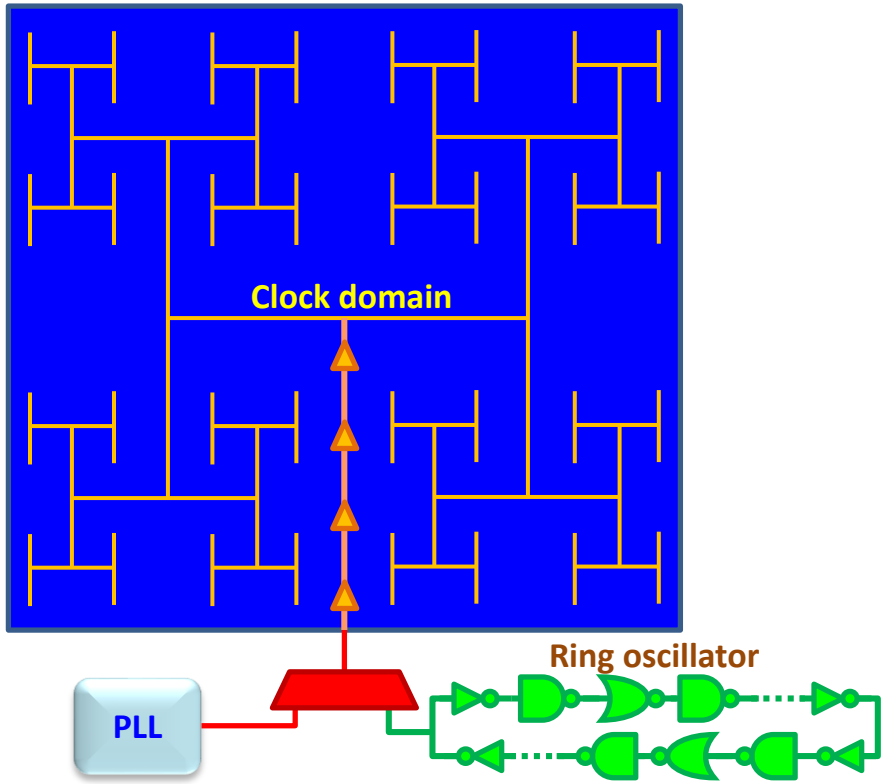
$$\frac{\sigma_{RO}^2}{\mu_{RO}} \simeq \frac{\sigma_{CP}^2}{\mu_{CP}}$$

new derating factor

$$\mu_{RO} > \left(1 + \frac{\delta\sqrt{8 + \delta^2} + \delta^2}{2}\right)\mu_{CP}$$

For small values of δ → $\mu_{RO} > (1 + \delta\sqrt{2})\mu_{CP}$

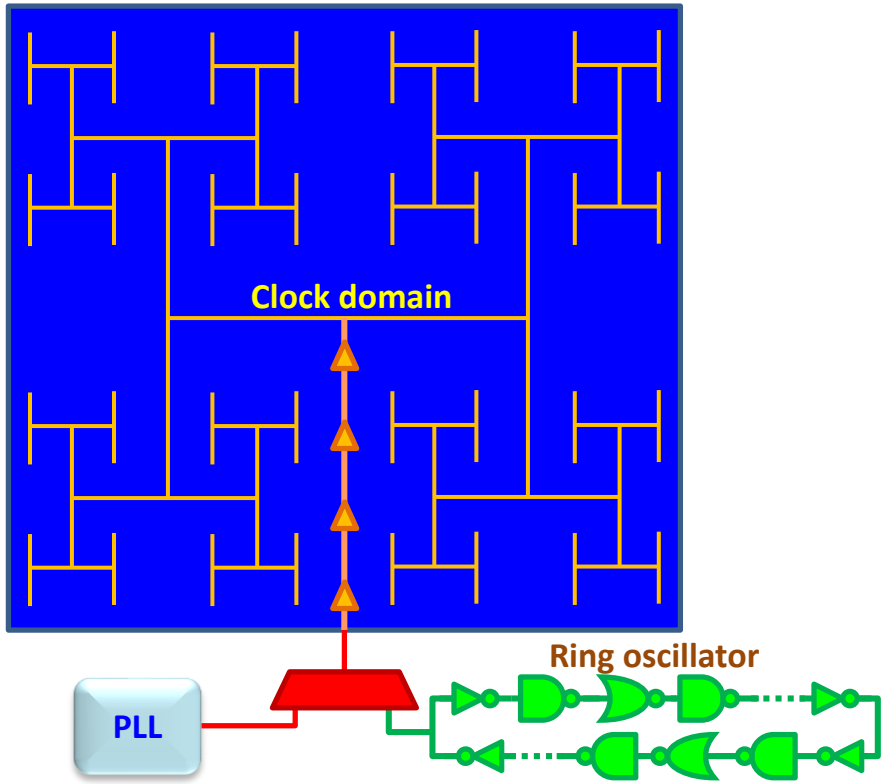
Apple-to-apple comparison



$$\texttt{PLLperiod} > (1+\delta)\cdot\texttt{PathDelay} + \texttt{Jitter}$$

$$\texttt{ROdelay} > (1+\delta\sqrt{2})\cdot\texttt{PathDelay}$$

Apple-to-apple comparison



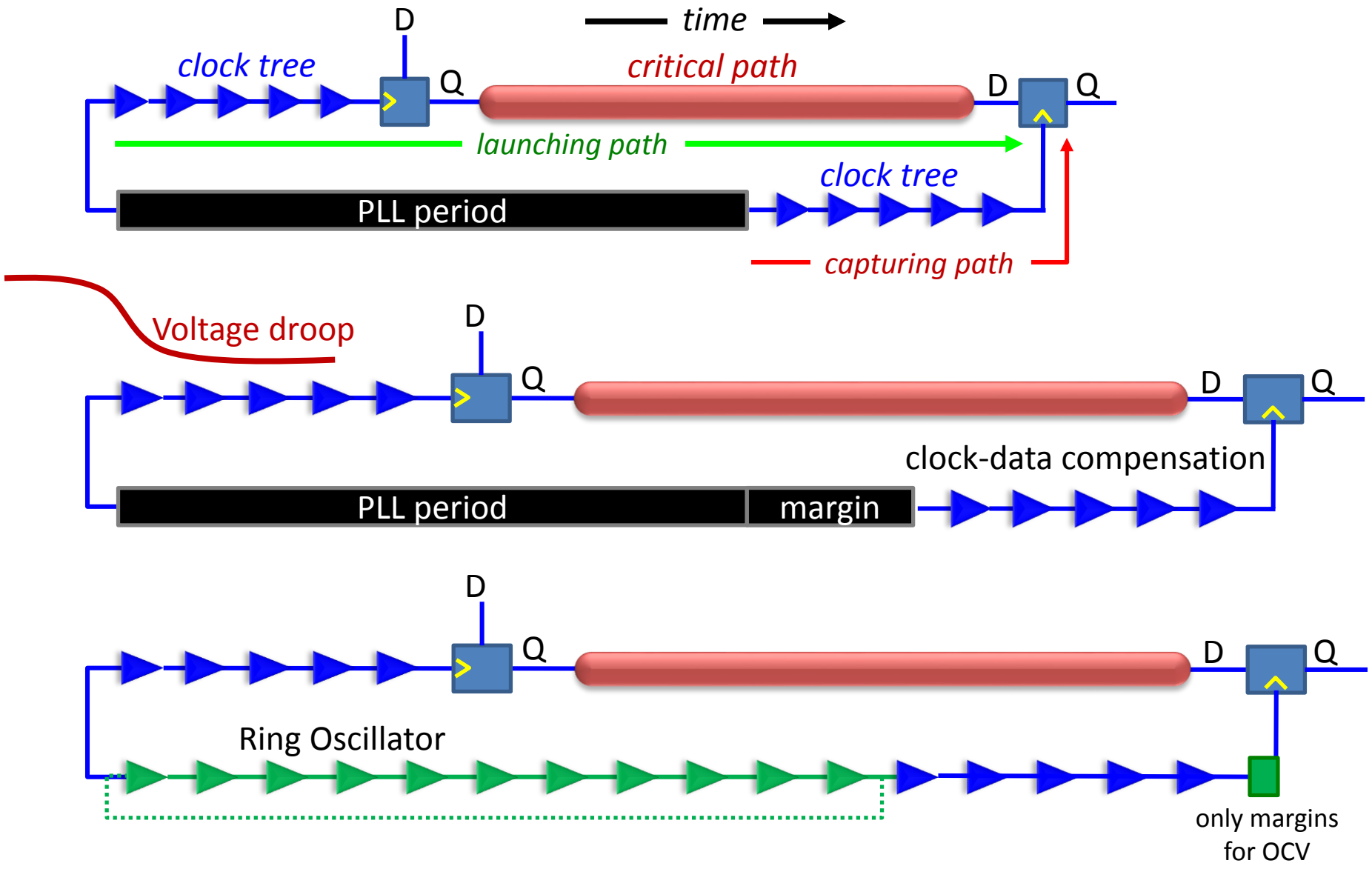
Fixed

$$\mathtt{PLLperiod} > 1.15 \cdot \mathtt{PathDelay} + \mathtt{Jitter}$$

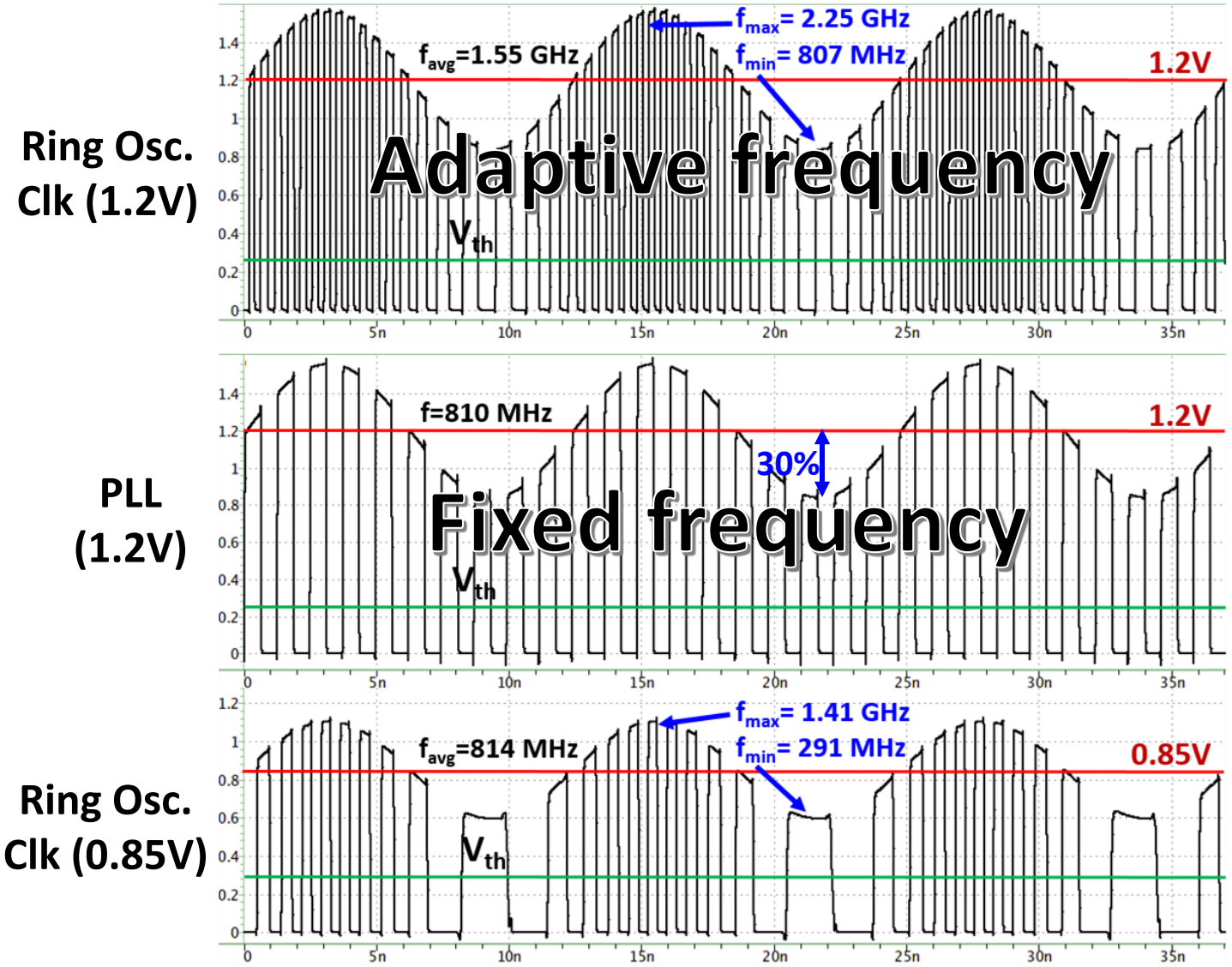
$$\mathtt{ROdelay} > 1.21 \cdot \mathtt{PathDelay}$$

Adaptive !!!

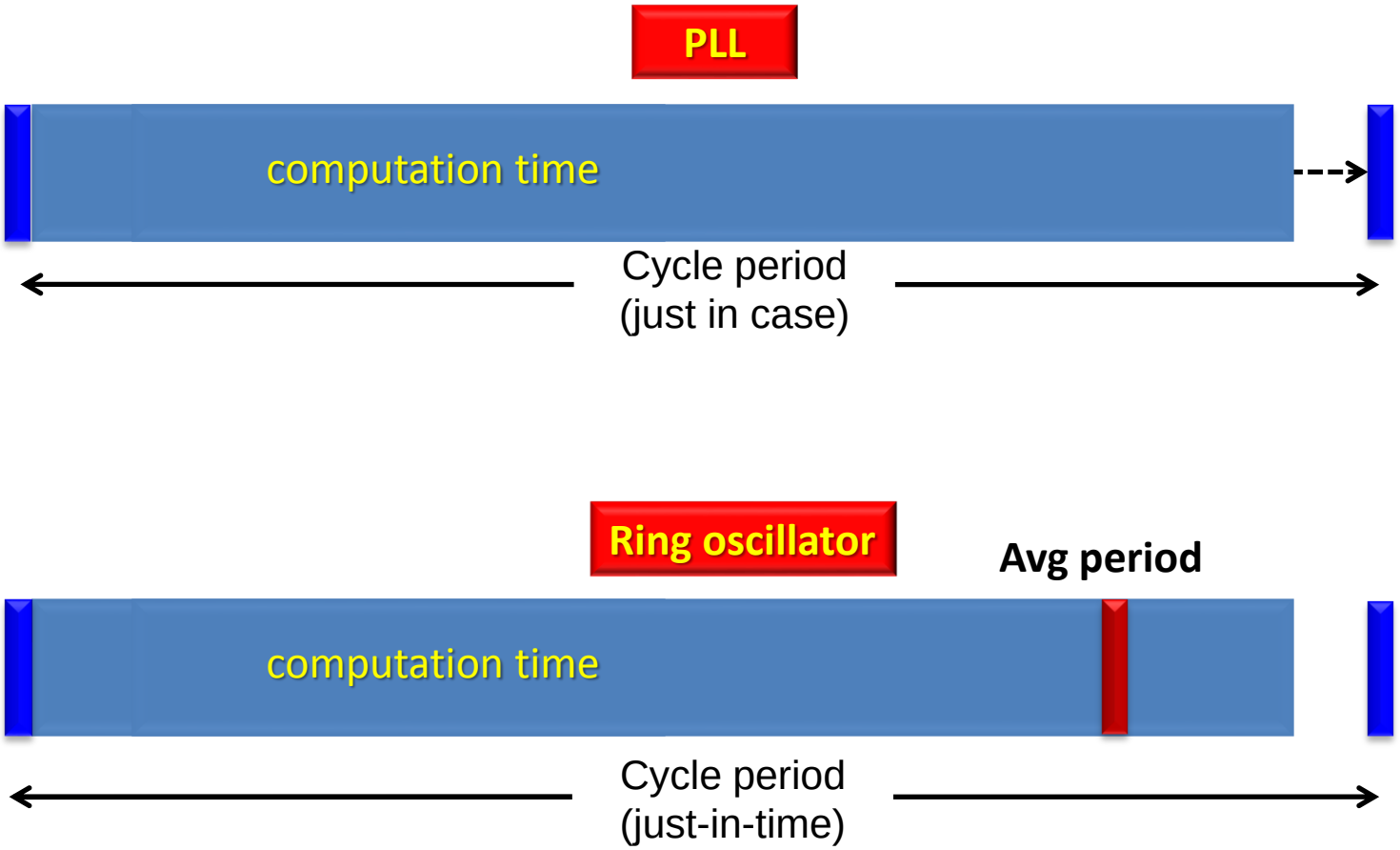
Variability: PLL vs. Reactive Clock



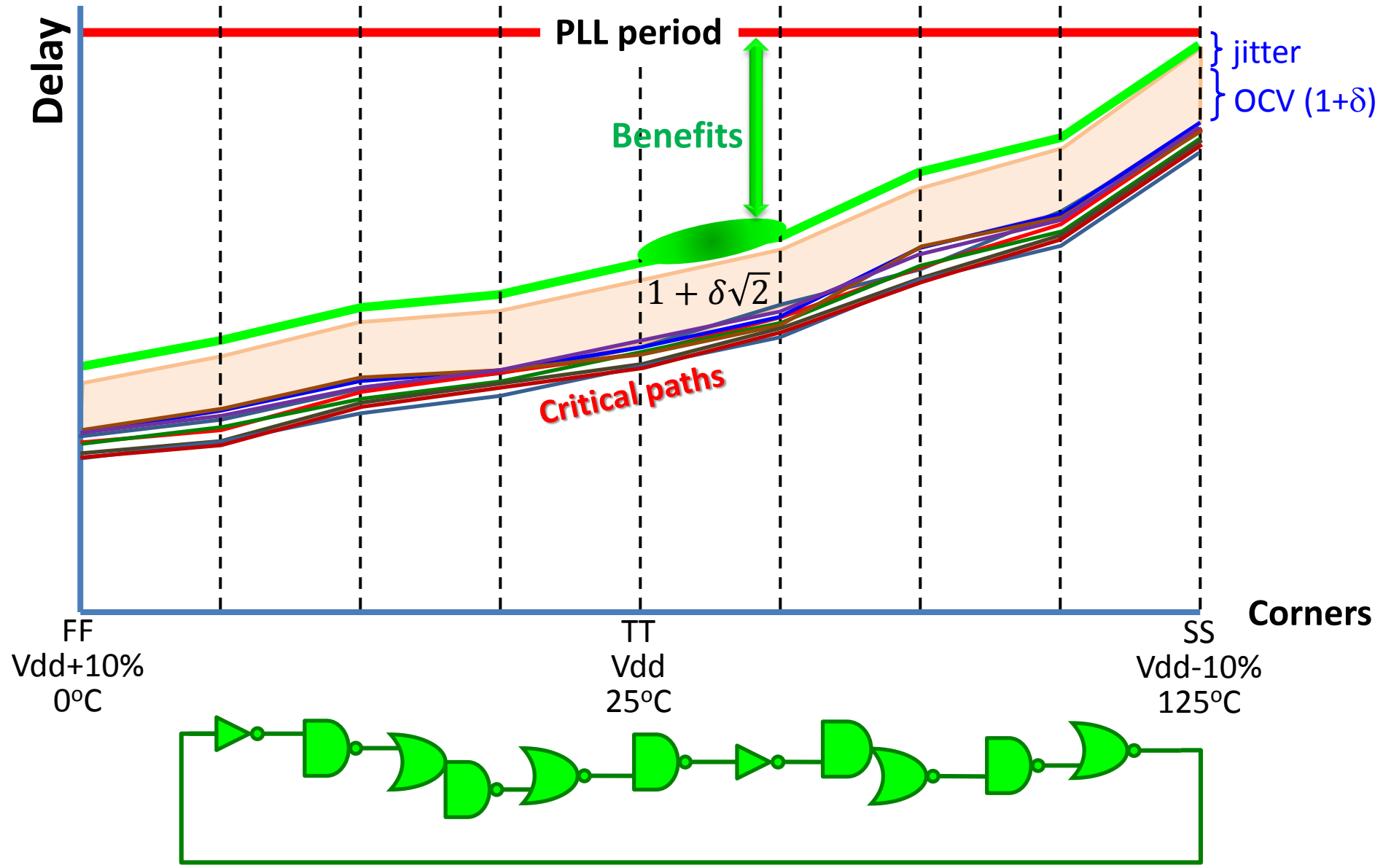
PLL vs. Ring Oscillator



PLL vs. Ring Oscillator

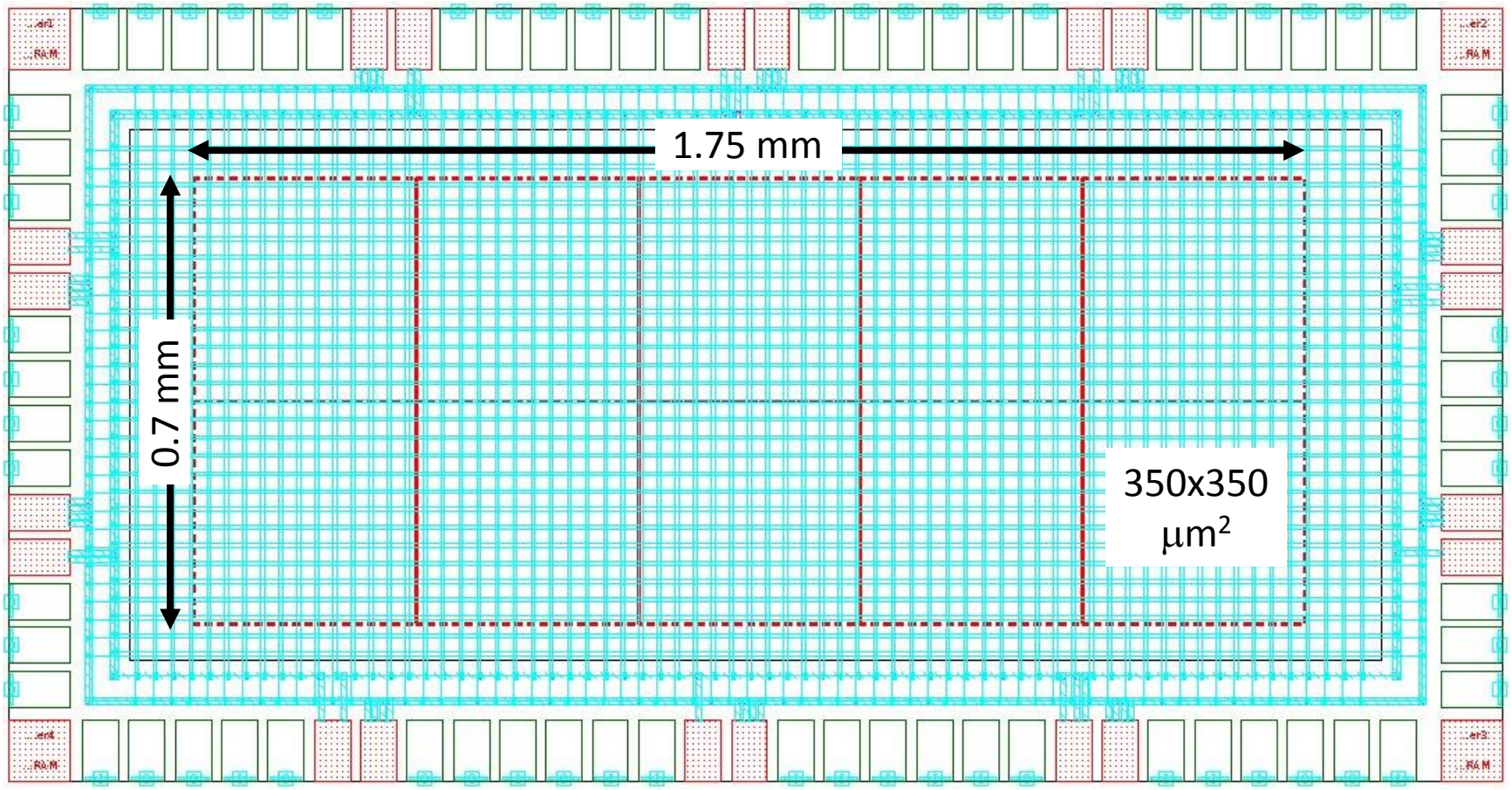


Synthesis of the Ring Oscillator



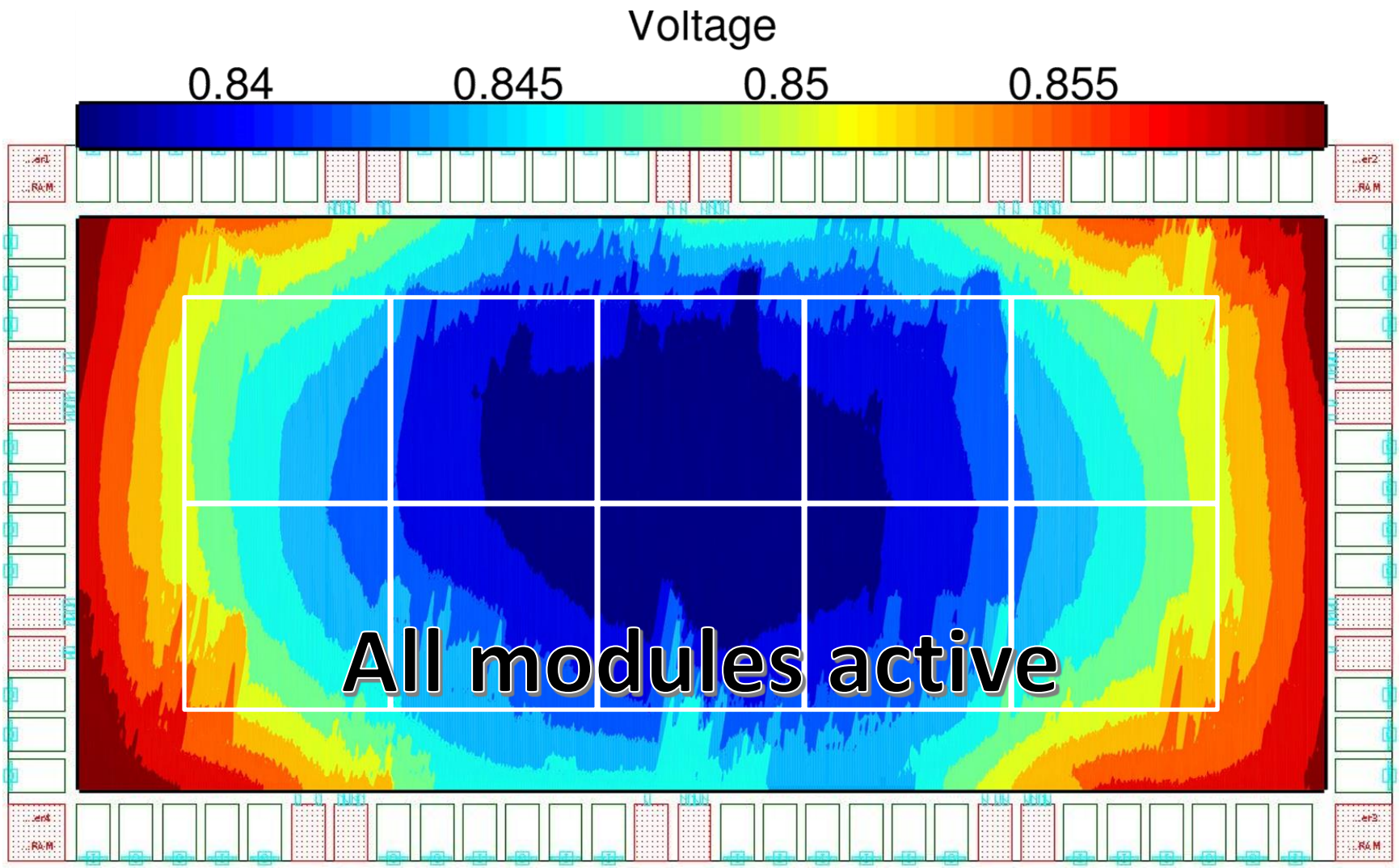
Experiment

10 AES modules (65nm)



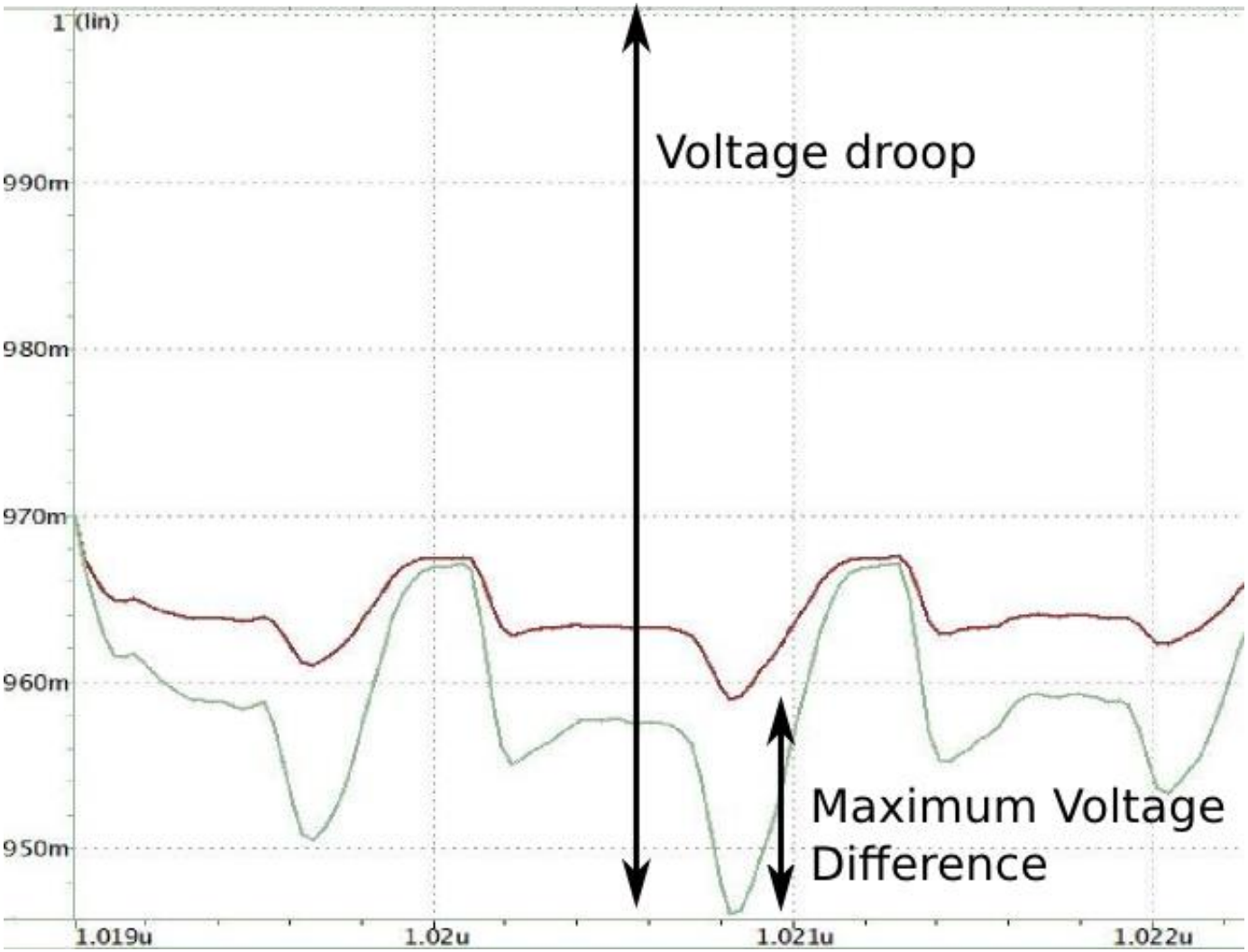
Every AES module can be activated/deactivated by clock gating
Switching activity generated by VCS
IR drop (static and dynamic) estimated by PrimeRail

Voltage droop analysis

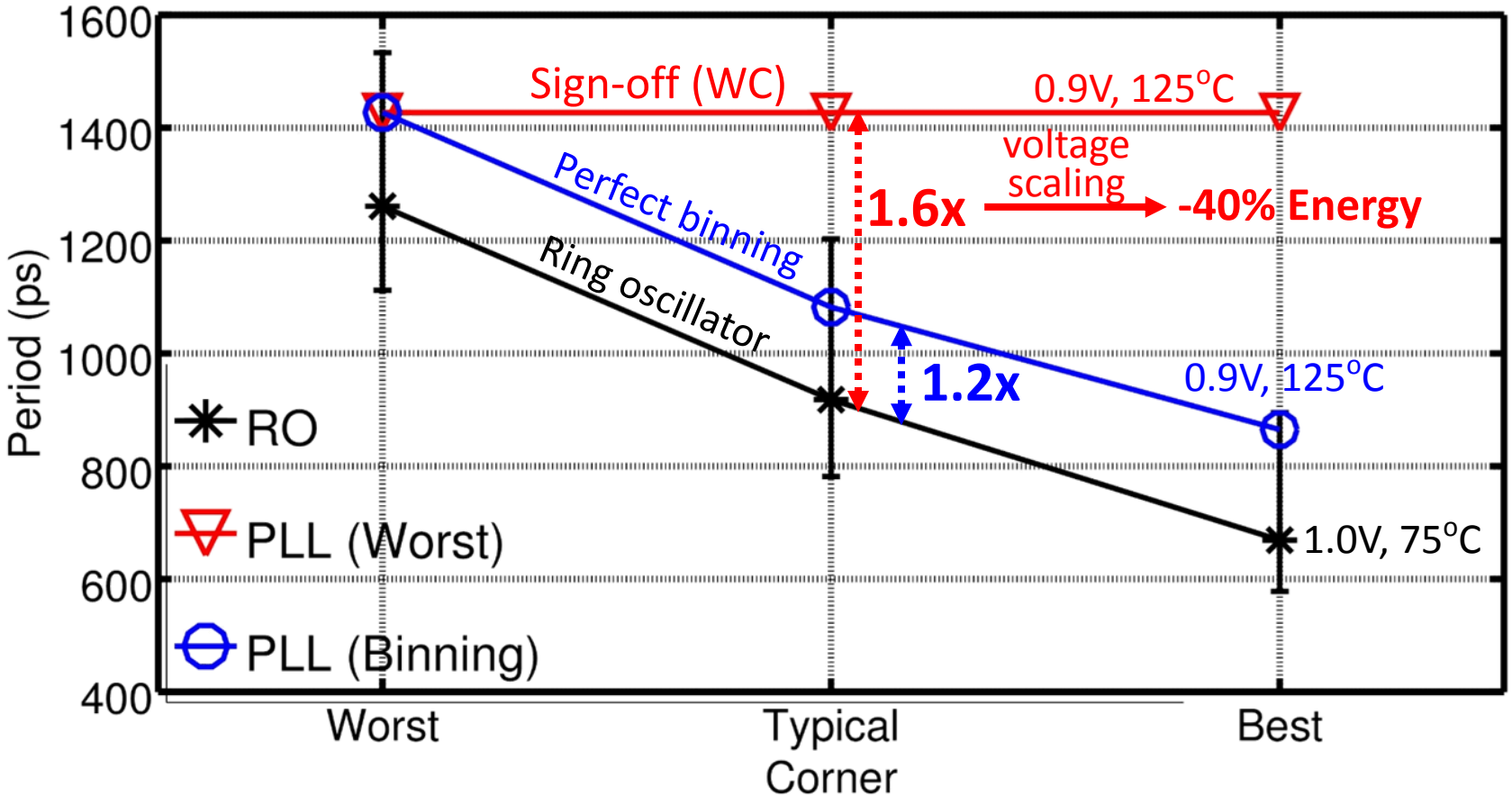


Nominal voltage: 1V Max voltage droop: 168mV Max voltage difference: 25mV

Max voltage difference



Performance & Energy benefits



Reactive Clocks

J. Cortadella, L. Lavagno, P. López, M. Lupon, A. Moreno, A. Roca and S.S. Sapatnekar
Reactive Clocks with variability-tracking jitter
ICCD 2015.

- Algorithms and EDA scripts for timing analysis:
  - Automatic synthesis of Ring Oscillators
  - Technology independent (any .lib file)
  - Adaptable to different STA and P&R tools

- Ring Oscillators + monitors for *post-silicon calibration*:
  - Non-intrusive monitors automatically synthesized
  - Patented technology

Conclusions

- Moore's law is (economically) over. It's time to exploit what is left in established nodes.

- *Ring Oscillators*: a zero-risk scheme to
  - boost performance (1.6x speedup) or
  - reduce energy (40%)

- Margins for Ring Oscillators (or matched delays)
  - Use the same library corners
  - Derating factor: $(1+\delta) \rightarrow (1+\delta\sqrt{2})$