Fault Classification of the Error Detection Logic in the Blade Resilient Template

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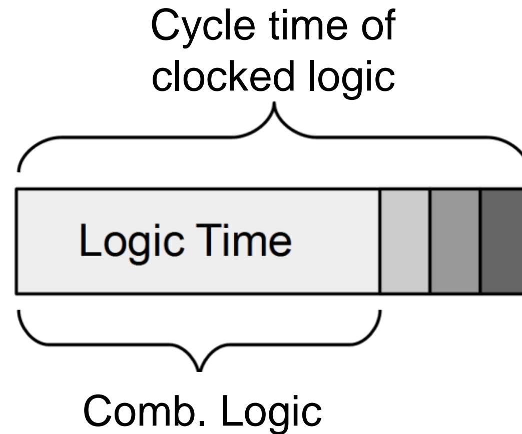
Delay Overheads

- Delay margins limits performance gains and increase power consumption



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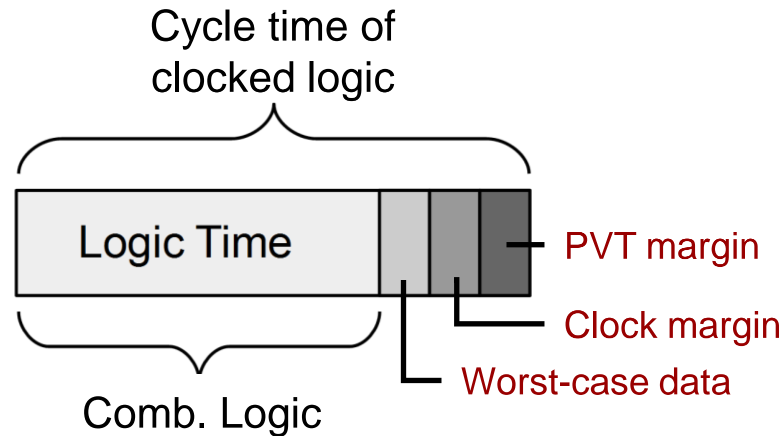

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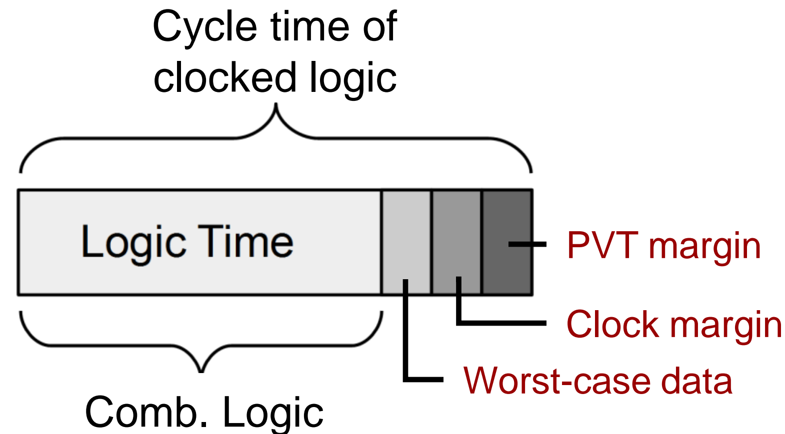

- Increase desire to operate near threshold voltage levels
  - Challenging in technologies like 45nm, 28nm and below due to PVT

Resilient Design

- Resilient design emerged as a solution to reduce timing margins

- Allow the circuit to operate with relaxed timing constraints
  - Extra logic to detect and recover from timing violations

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- Past synchronous resilient designs
  - Metastability issues
  - High recovery penalties

Resilient Design

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  - 30% power reduction at the same performance for a 10% area overhead
- Why resilient designs are not widely used?
- Challenges in terms of testability

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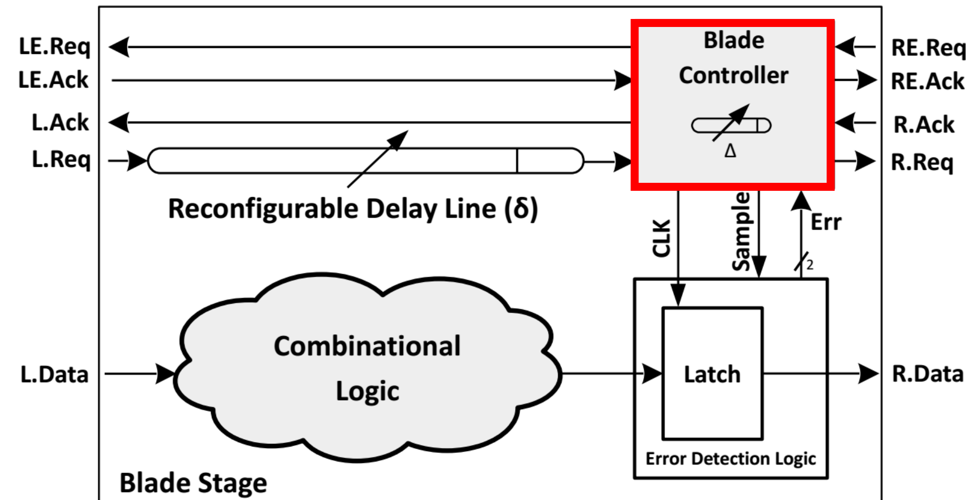
  - Pass/fail criteria needs to be re-examined
- Limited chip area for test circuitry
  - Area overhead may be critical
- Is functional test enough?
- Can we use existing error detection logic for testing?

Outline

- Blade Template
- Simulation Environment
- EDL Fault Classification
- EDL Fault Analysis
  - Stuck-at Faults
  - Delay Faults
- Conclusions and Next Steps

Blade Template

- Blade controller
  - Two 2-phase BD channels
    - L and R
    - LE and RE



[Hand et al., ASYNC 2015]

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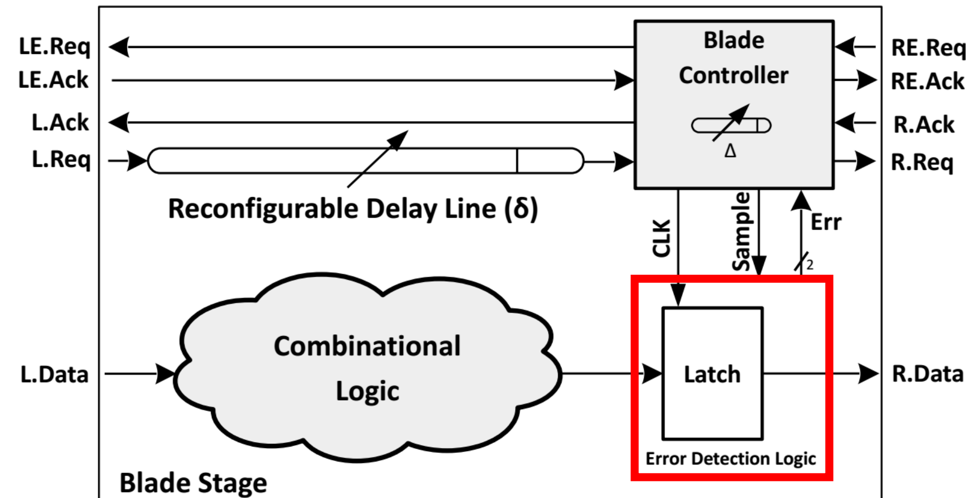

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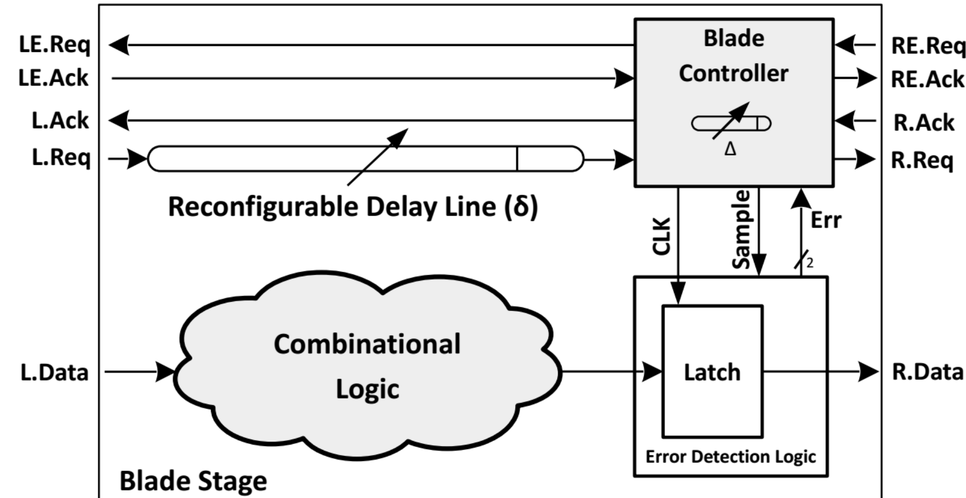

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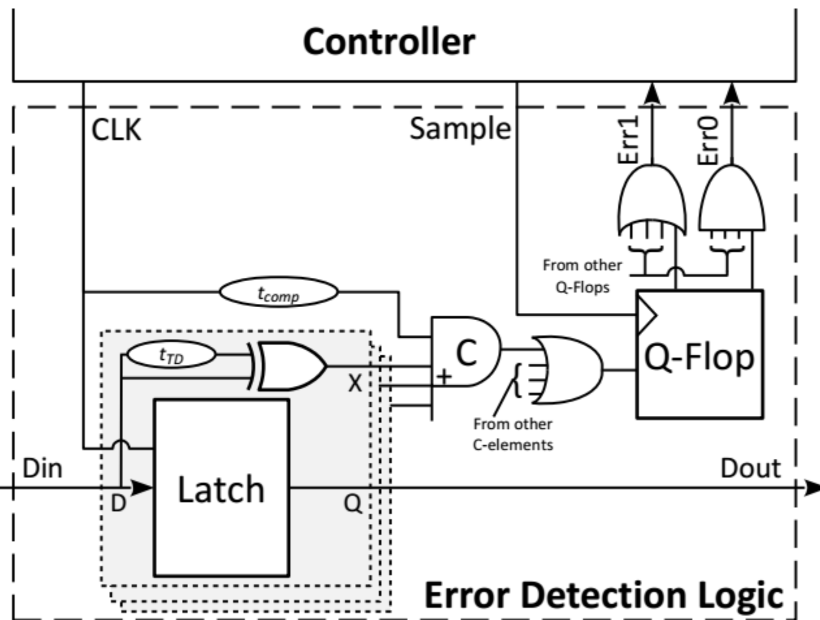
- Two reconfigurable delay lines
  - δ time where data can be propagate through the EDL
  - Δ time that the latch is transparent

Error Detection Logic



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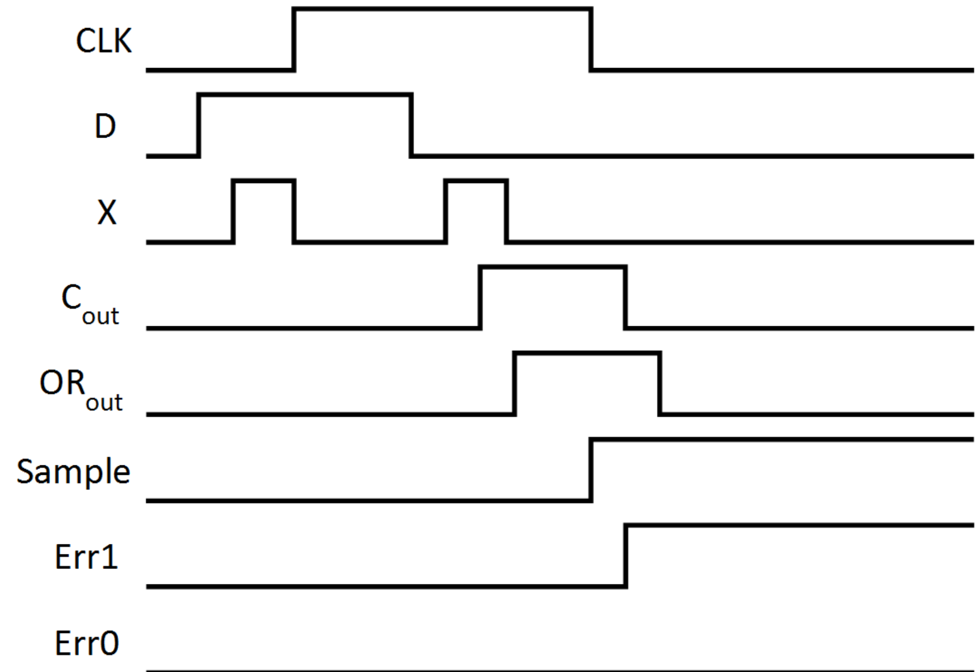

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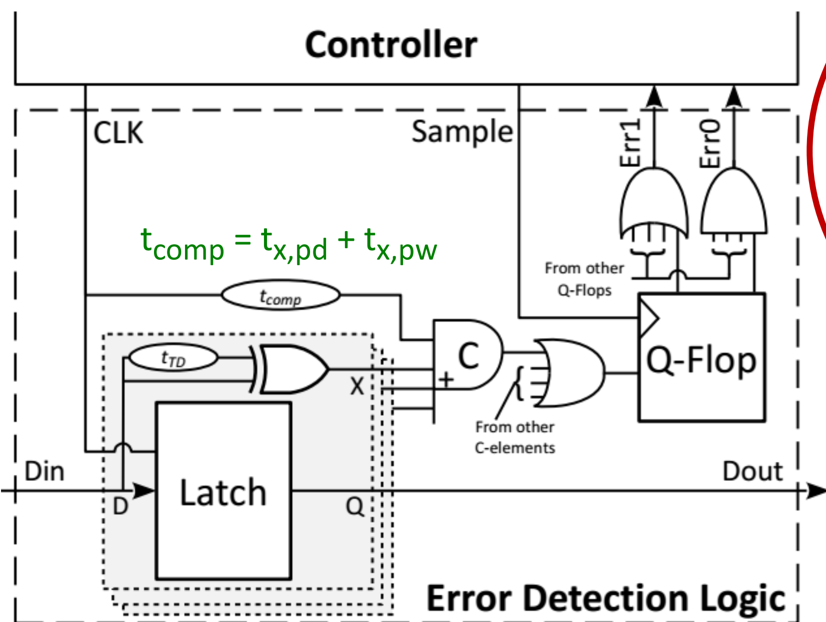

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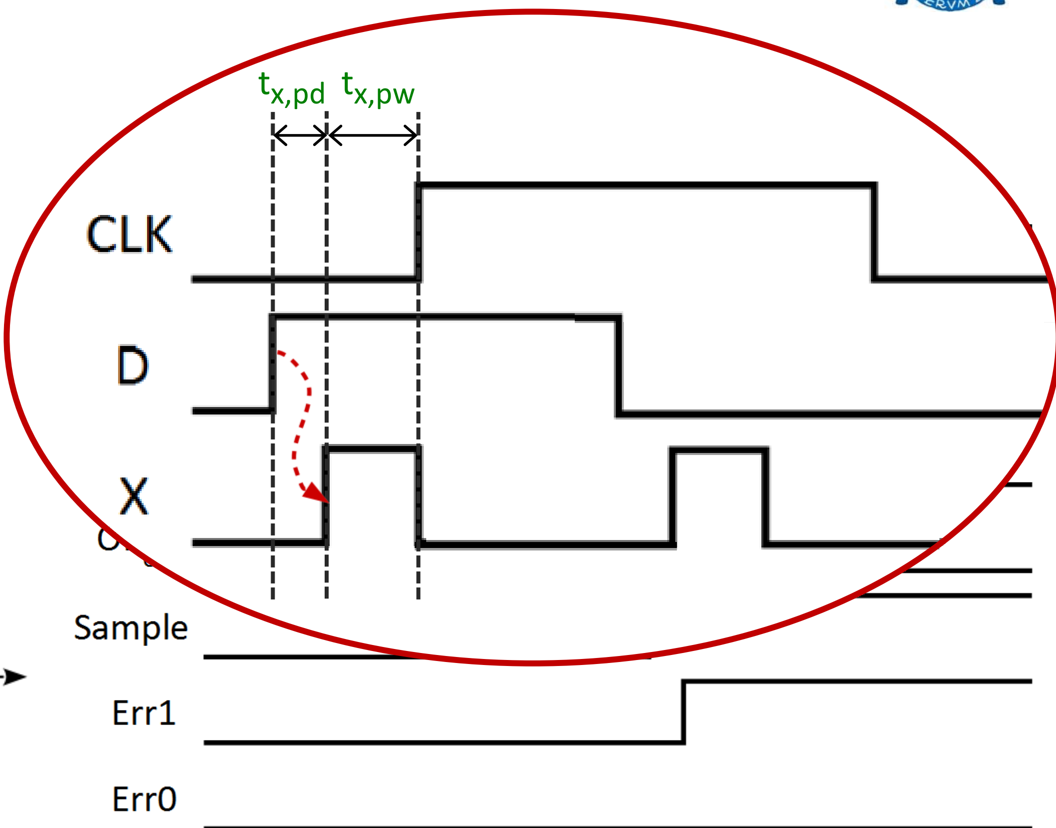

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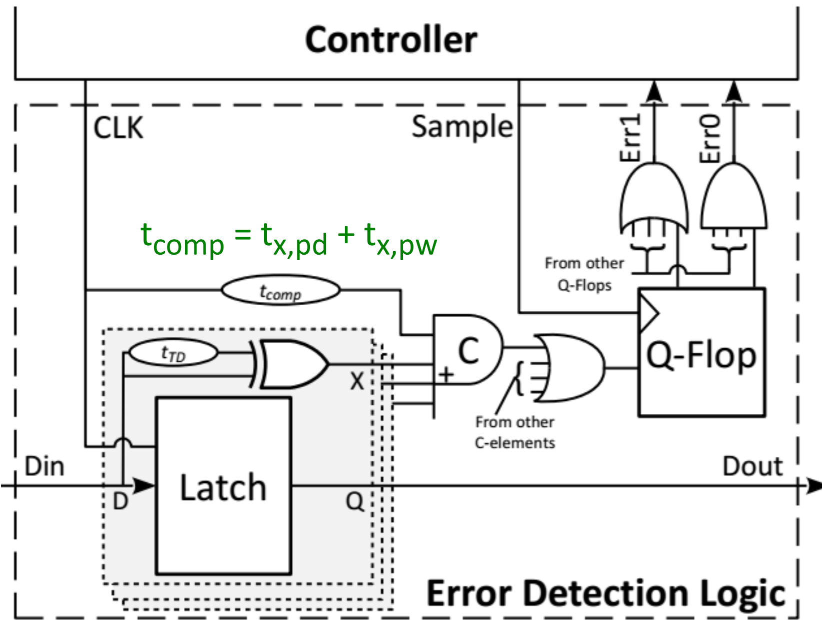

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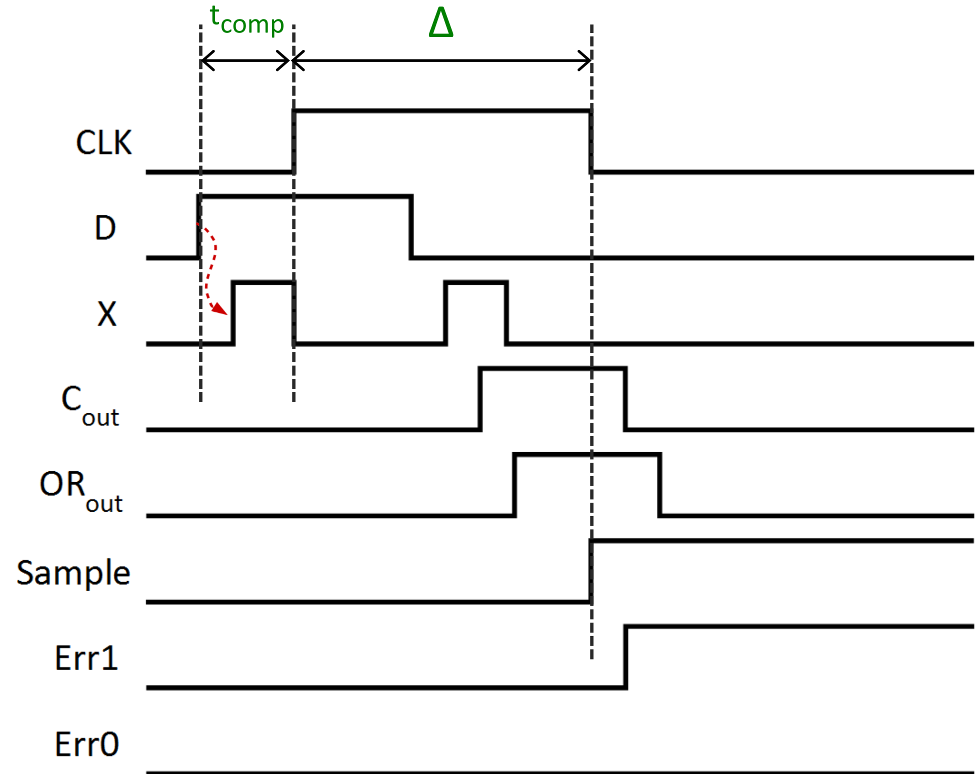

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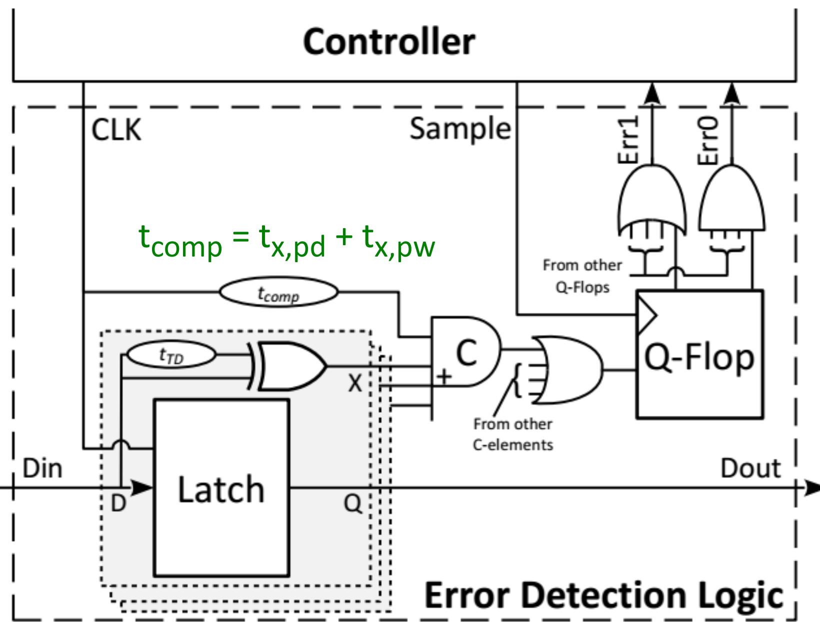


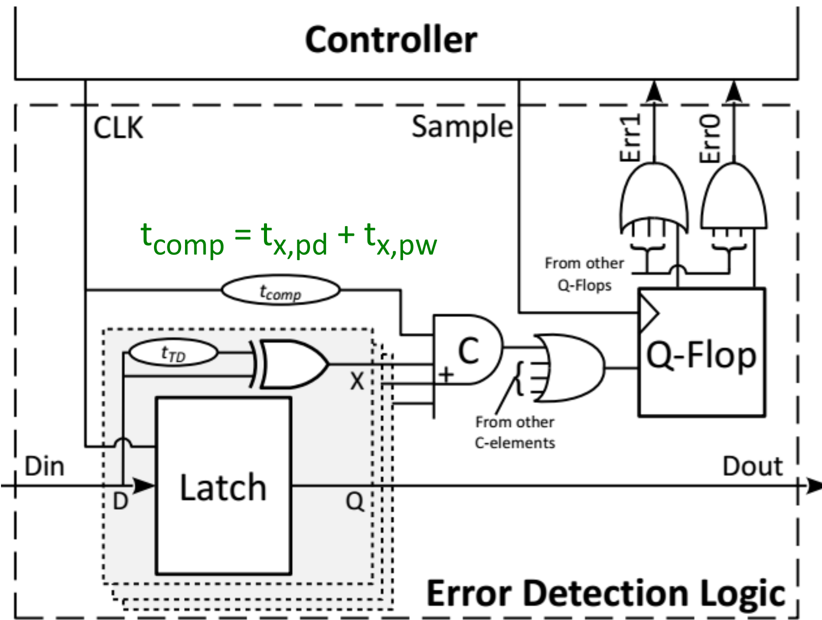
[Hand et al., ASYNC 2015]

$t_{CE,pd}$ +
$t_{OR,pd}$ +
$t_{QF,setup}$

t_{comp}

CLK
D
X
C_{out}
OR_{out}
Sample
Err1
Err0

Error Detection Logic



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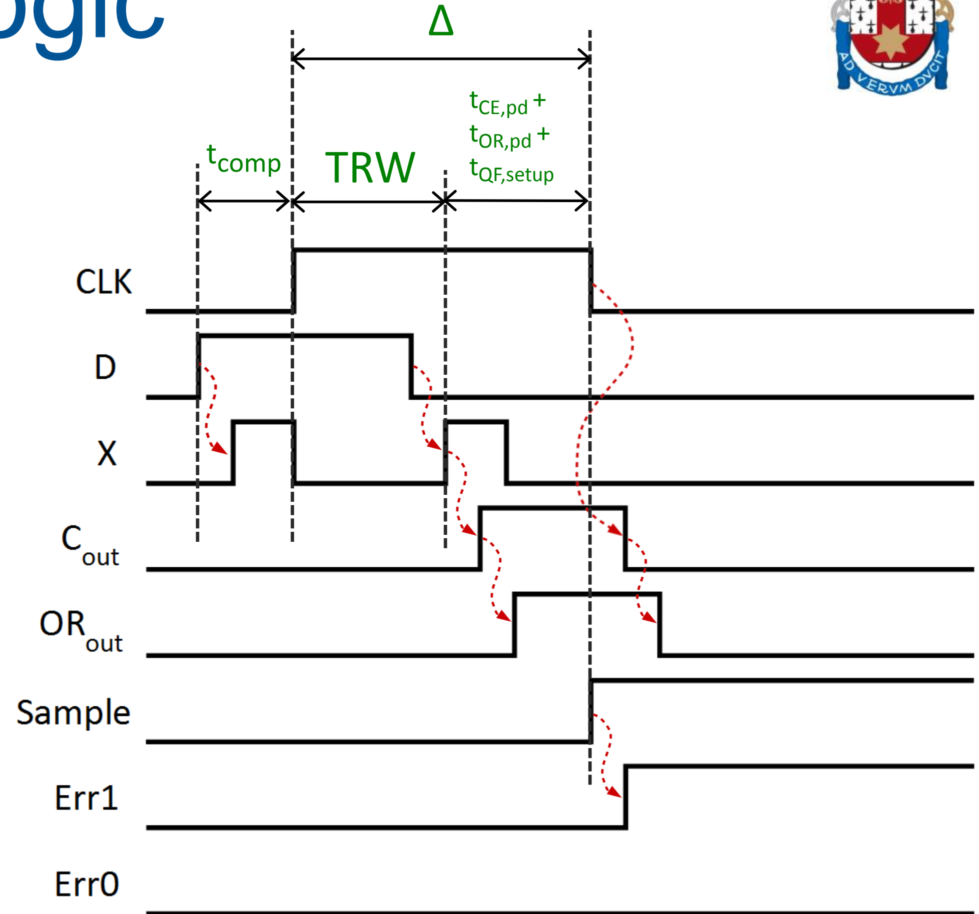

$$TRW = \Delta + t_{X,pw} - (t_{CE,pd} + t_{OR,pd} + t_{QF,setup})$$

Simulation Environment

- Two types of faults are considered
  - Stuck-at faults
    - Wires stuck-at-0 (ST0) stuck-at-1 (ST1)
  - Delay faults
    - Longer propagation delay (LPD)
    - Shorter propagation delay (SPD)

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  - Delay faults
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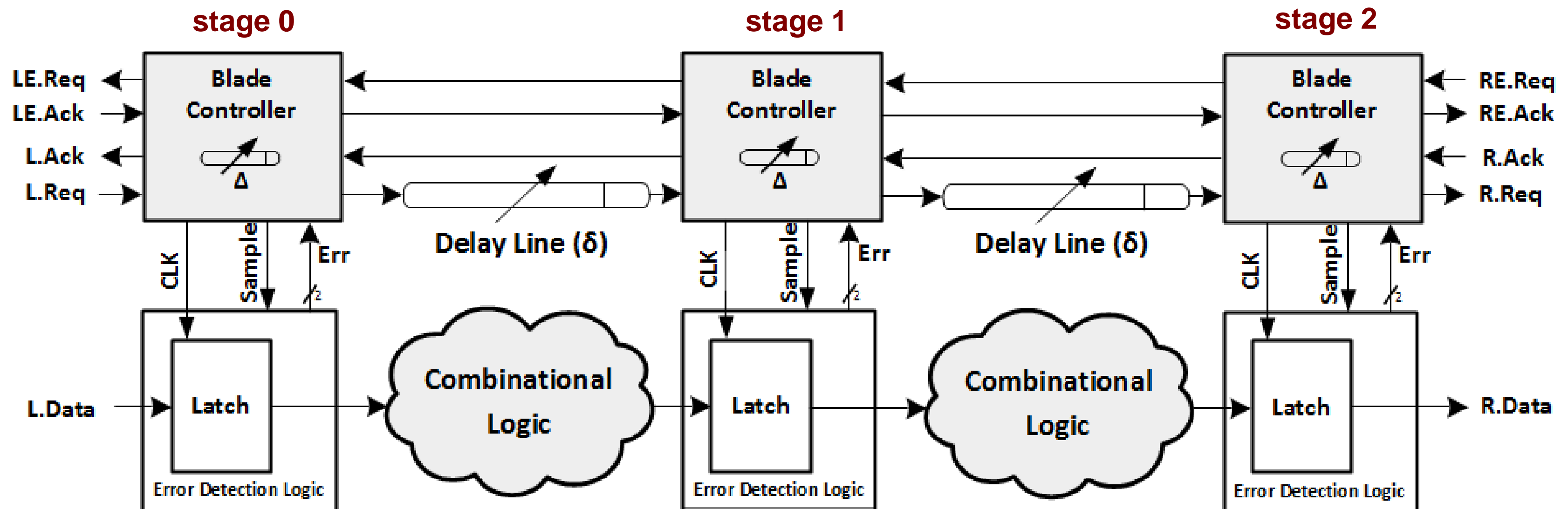
    - Shorter propagation delay (SPD)
- Only single faults are considered
- Data is not masked between stages

Simulation Environment

- 3 stage pipeline



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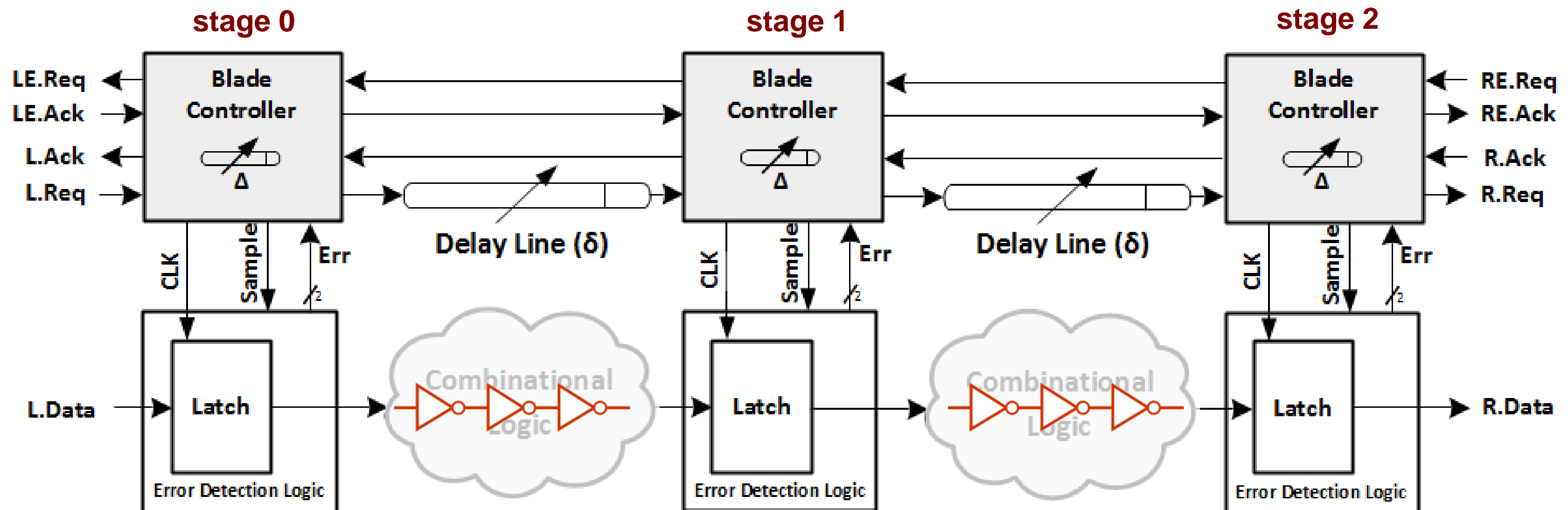
- 3 stage pipeline
  - Dummy combinational logic – balanced stages
  - Timing violations (TV) by extending the inverters delay



Simulation Environment

- 3 stage pipeline
  - Dummy combinational logic – balanced stages
  - Timing violations (TV) by extending the inverters delay
- Faults are inserted only in stage 1
- Error signals are observable

stage 0
stage 1
stage 2
LE.Req
LE.Ack
L.Ack
L.Req
Blade Controller
Δ
Delay Line (δ)
RE.Req
RE.Ack
R.Ack
R.Req
CLK
Sample
Err
2
L.Data
Latch
Error Detection Logic
Combinational Logic
R.Data

Fault Classification

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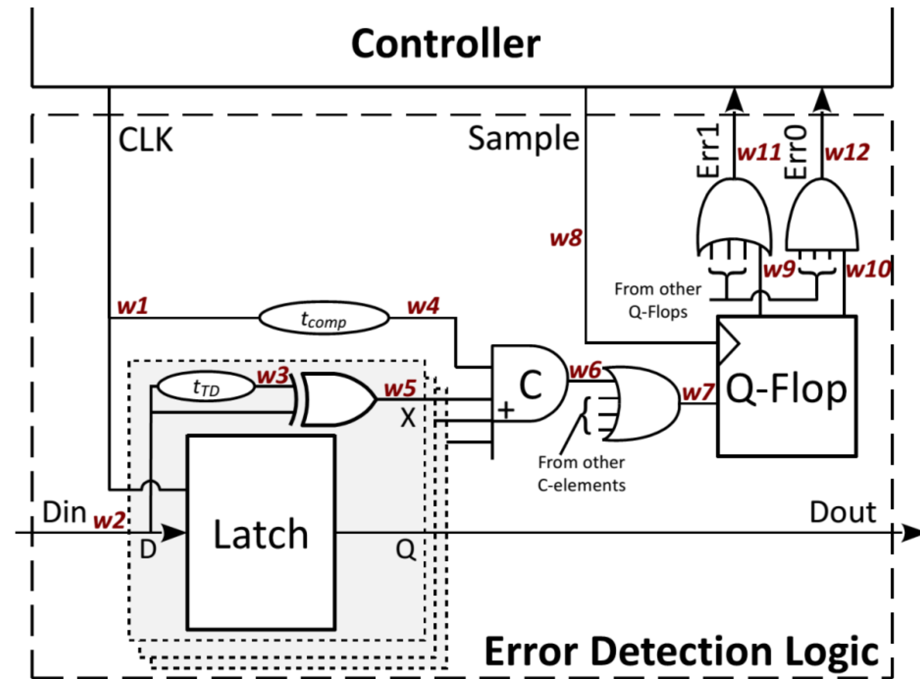
- Fault classification for stuck-at fault model

Faulty Line	SA0		SA1	
	wo/ TV	w/ TV	wo/ TV	w/ TV
$w1$	PH	PH	PH	PH
$w2$	PST	PST	PST	PST
$w3$	ERR_ST	ERR_ST	ERR_ST	ERR_ST
$w4$	UN	ERR_NST	ERR_ST	ERR_ST
$w5$	UN	ERR_NST	ERR_ST	ERR_ST
$w6$	UN	ERR_NST	ERR_ST	ERR_ST
$w7$	UN	ERR_NST	ERR_ST	ERR_ST
$w8$	PH	PH	PH	PH
$w9$	UN	PH	PH	PH
$w10$	PH	PH	UN	PH
$w11$	UN	PH	PH	PH
$w12$	PH	PH	PH	PH



Fault Classification

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PST	pipeline output stuck at a value
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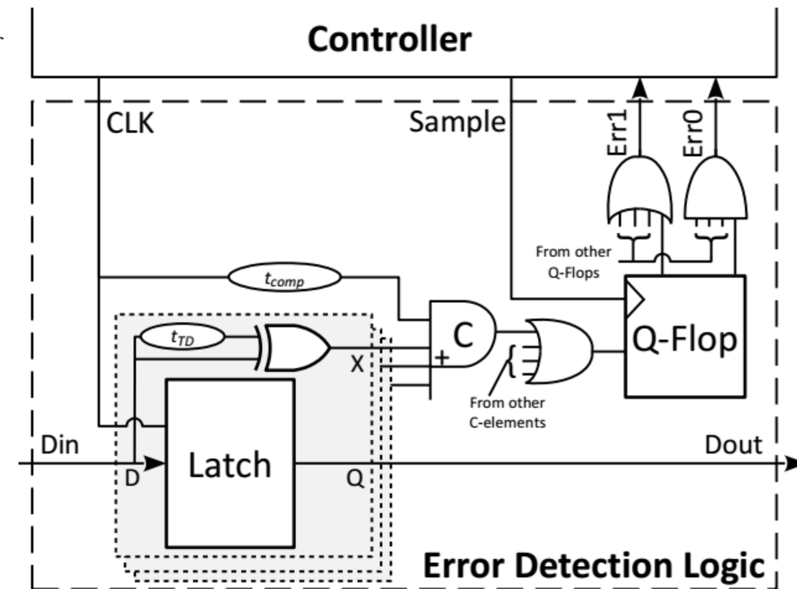
- Fault classification for delay fault model

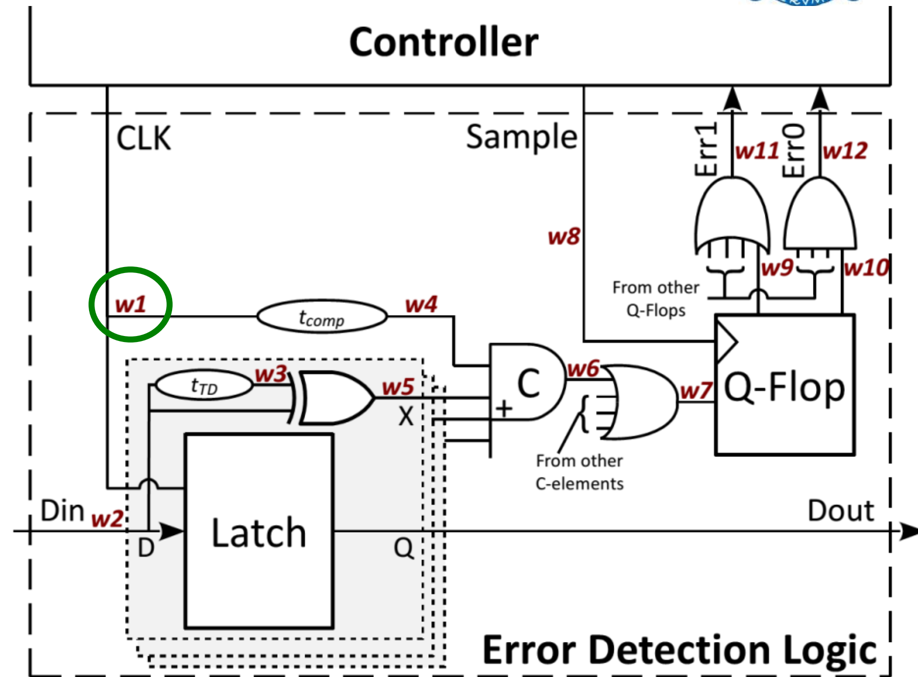
Faulty Element	SPD		LPD	
	wo/ TV	w/ TV	wo/ TV	w/ TV
Latch	-	-	ERR_NST	ERR_ST / ERR_NST
t_{comp}	ERR_ST	ERR_ST	UN	ERR_ST / ERR_NST
t_{TD}	UN	ERR_NST	ERR_ST	ERR_ST
XOR Gate	-	-	ERR_ST	ERR_ST
C-element	-	-	UN	ERR_NST
OR Gate	-	-	UN	ERR_NST
Q-Flop	-	-	-	-
OR Gate (Err1)	-	-	-	-
AND Gate (Err0)	-	-	-	-



Stuck-at Faults

w1

- SA0
  - Pipe halts (CLK never rises)
- SA1
  - Pipe halts (CLK never falls)



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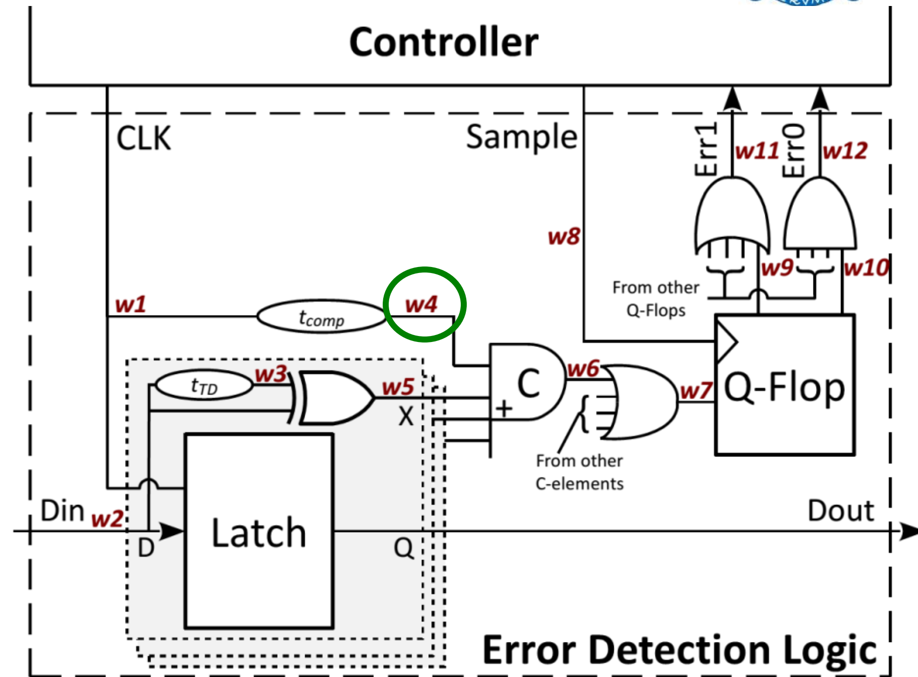


w1

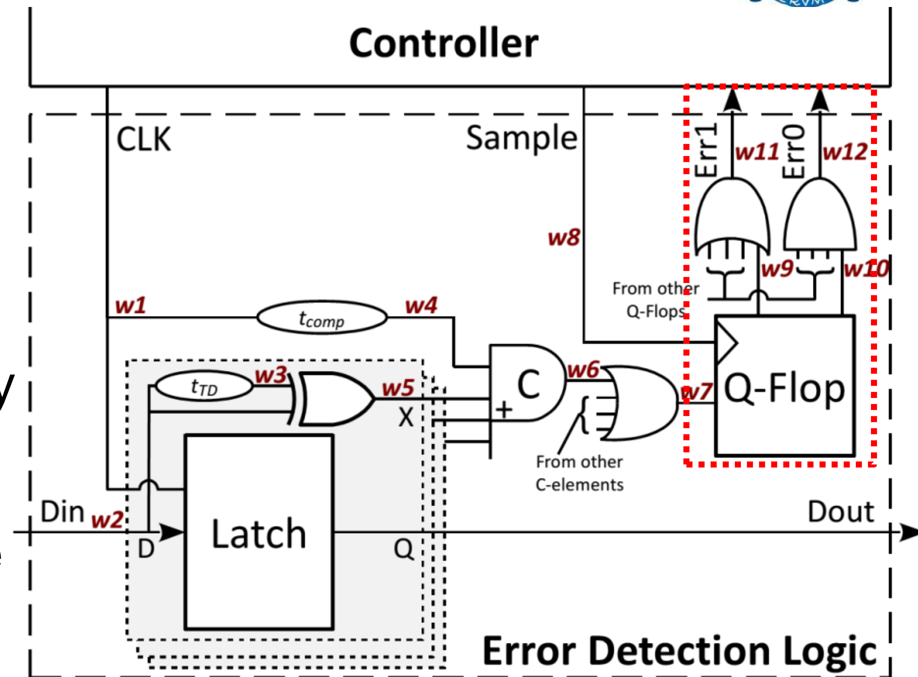
- SA0
  - Pipe halts (CLK never rises)
- SA1
  - Pipe halts (CLK never falls)

w4

- SA0
  - Error is never captured and TV propagated to the next stage
- SA1
  - Error is always generated, but circuit is still functional

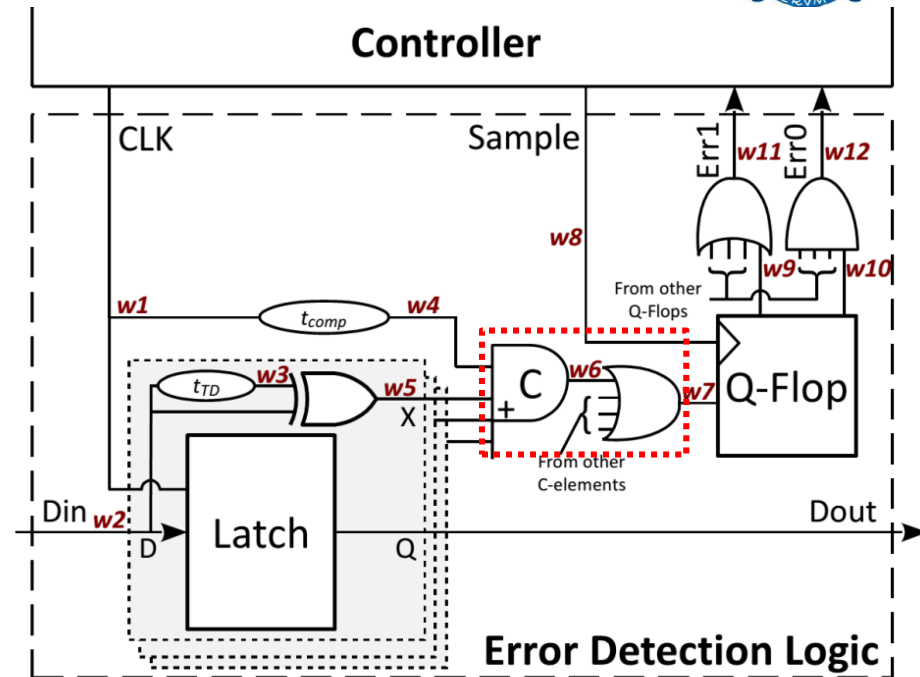
Delay Faults

- Q-Flop, OR and AND
  - SPD
    - It won't affect the functionality
  - LPD
    - Only affects the performance



Delay Faults

- C-element and OR Gate
  - LPD
    - Can miss a TV



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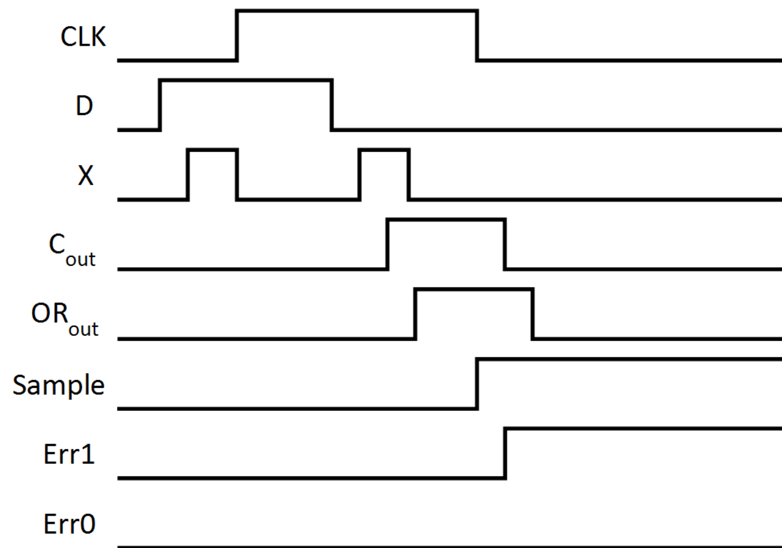

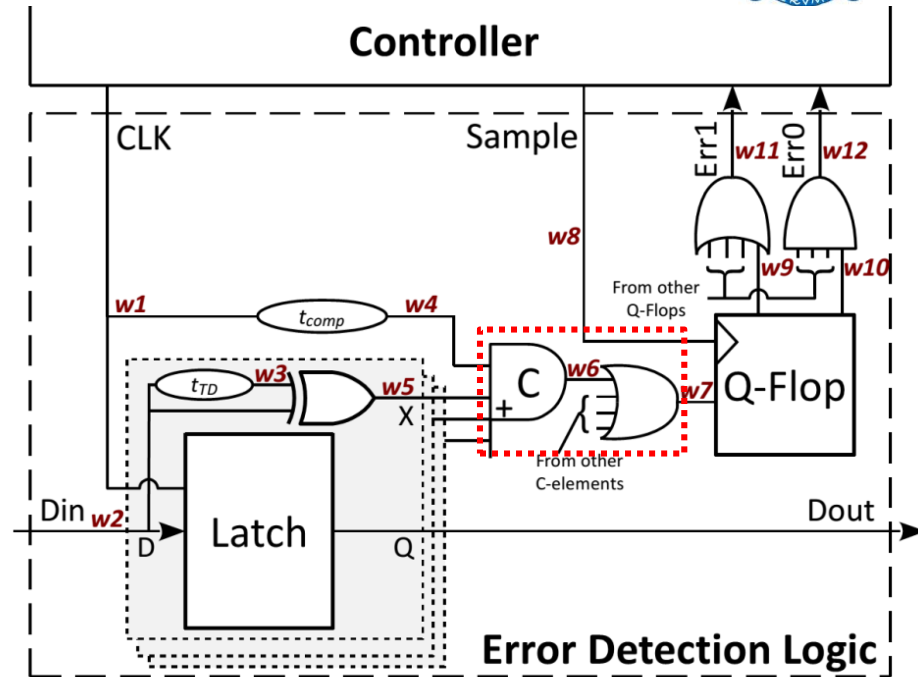

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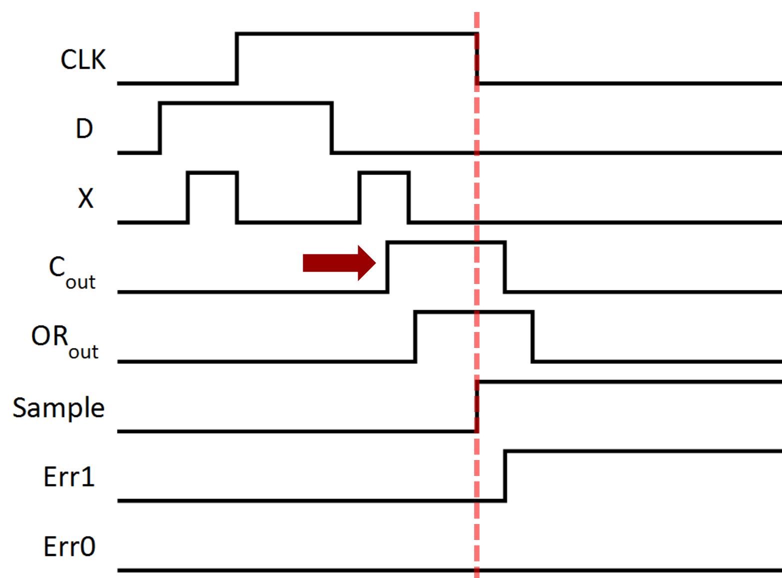

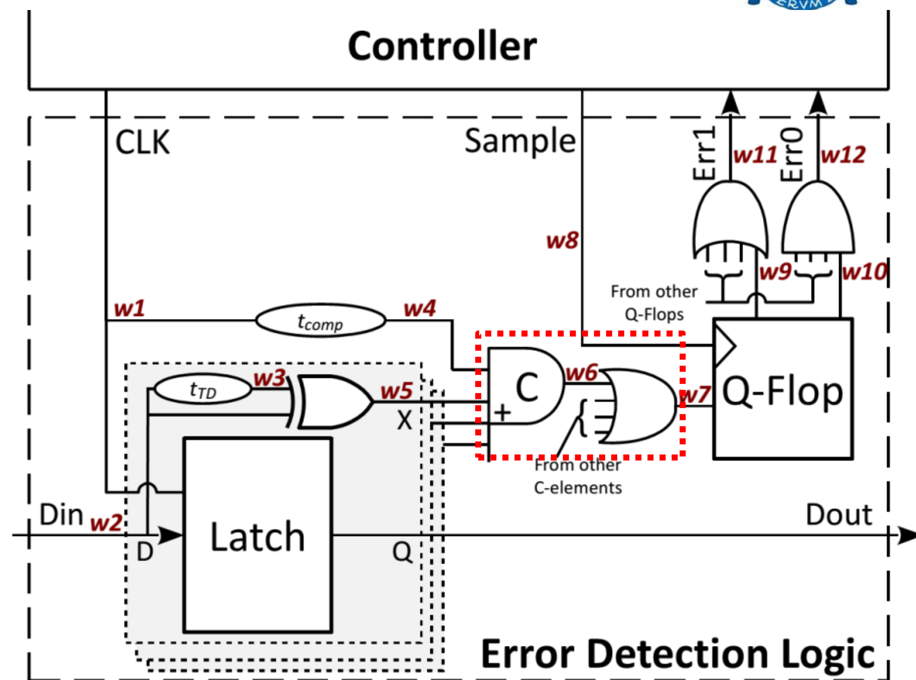

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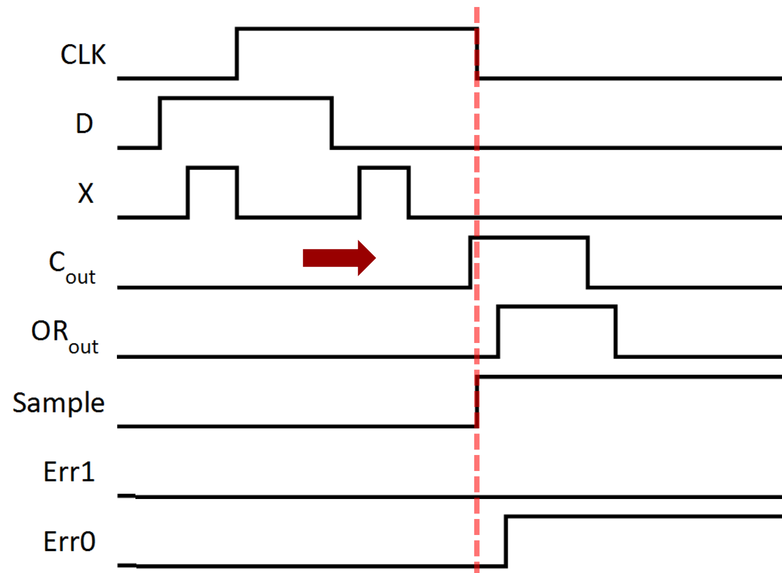
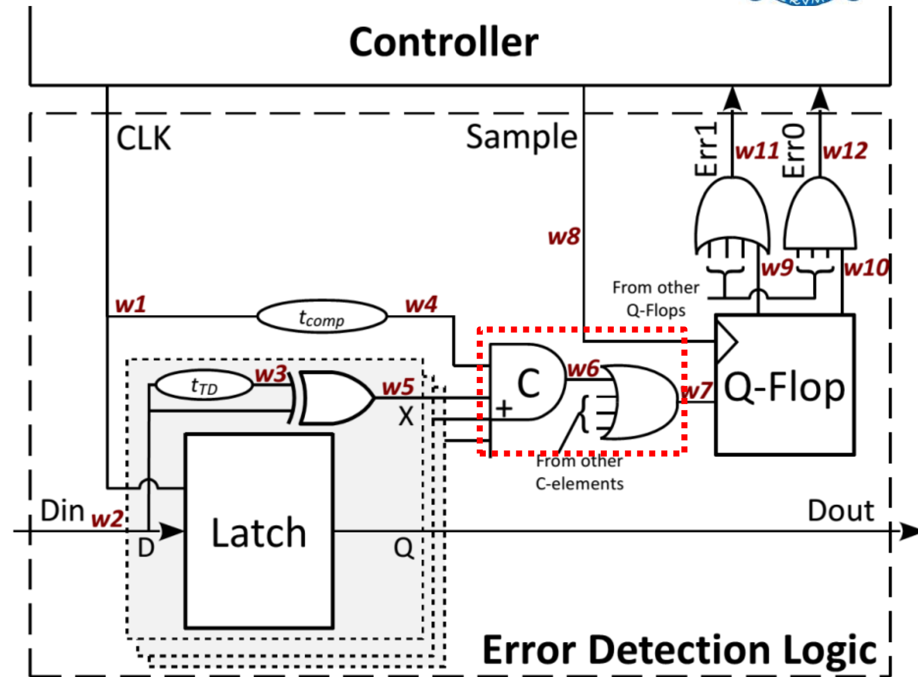
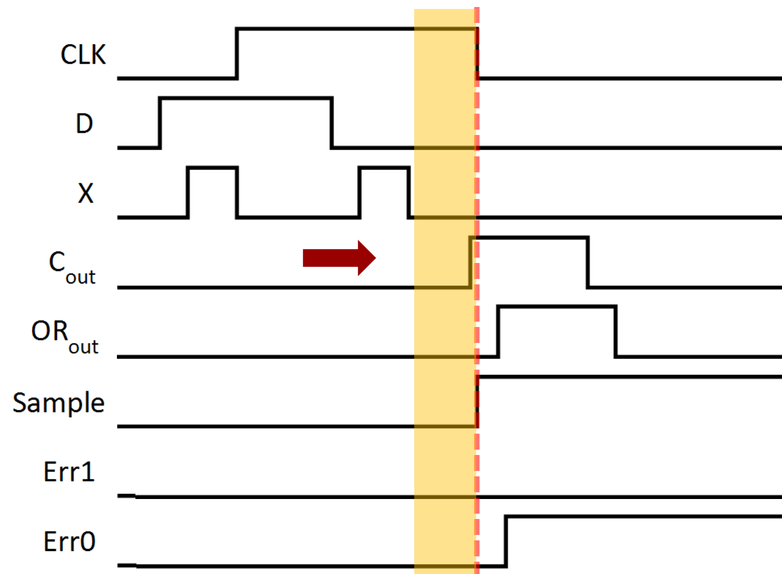
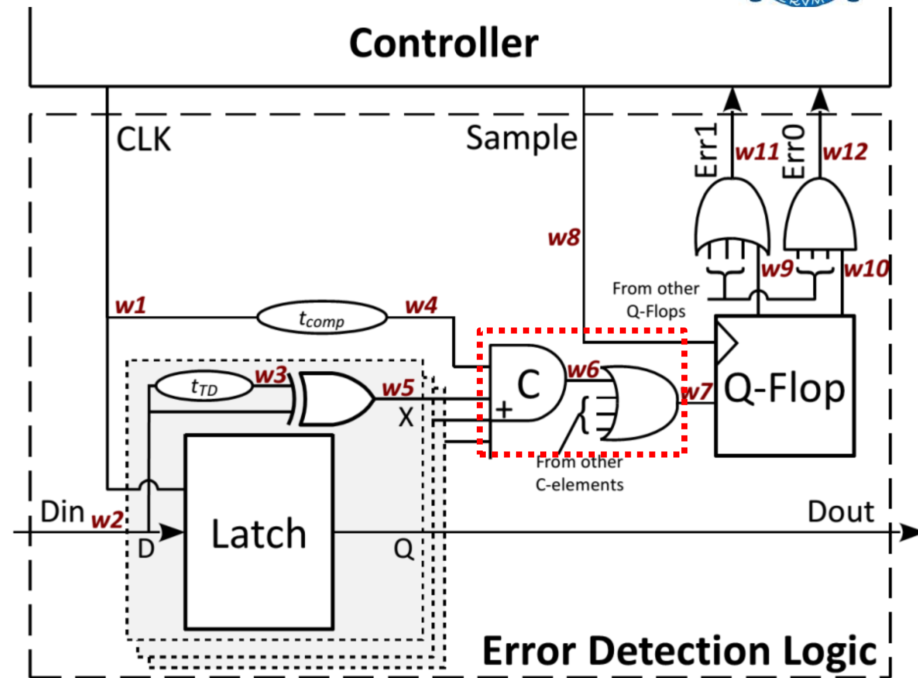




Delay Faults

- C-element and OR Gate
  - LPD
    - Can miss a TV
    - Captured by the next state

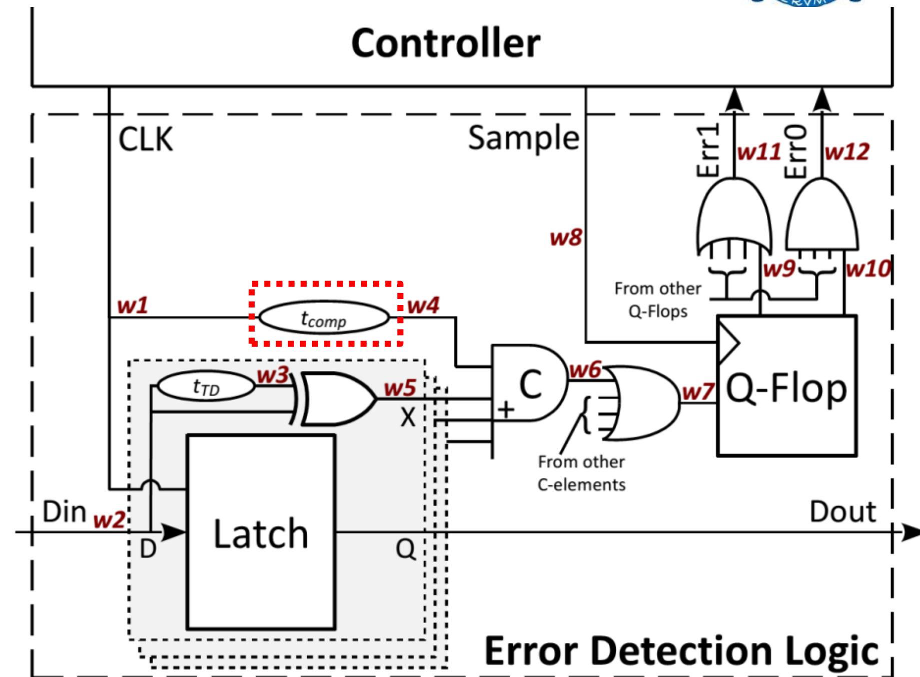




TV at the end
of TRW

Delay Faults

- Delay line – t_{comp}
  - LPD
    - Undetectable without a TV



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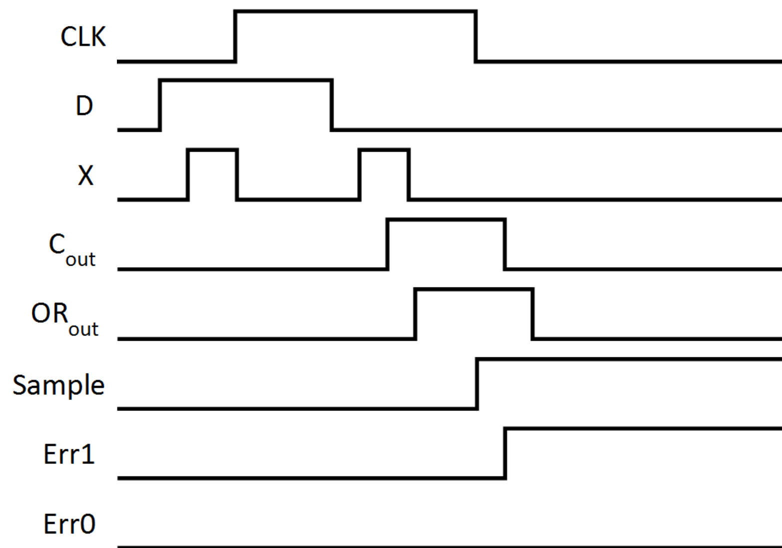

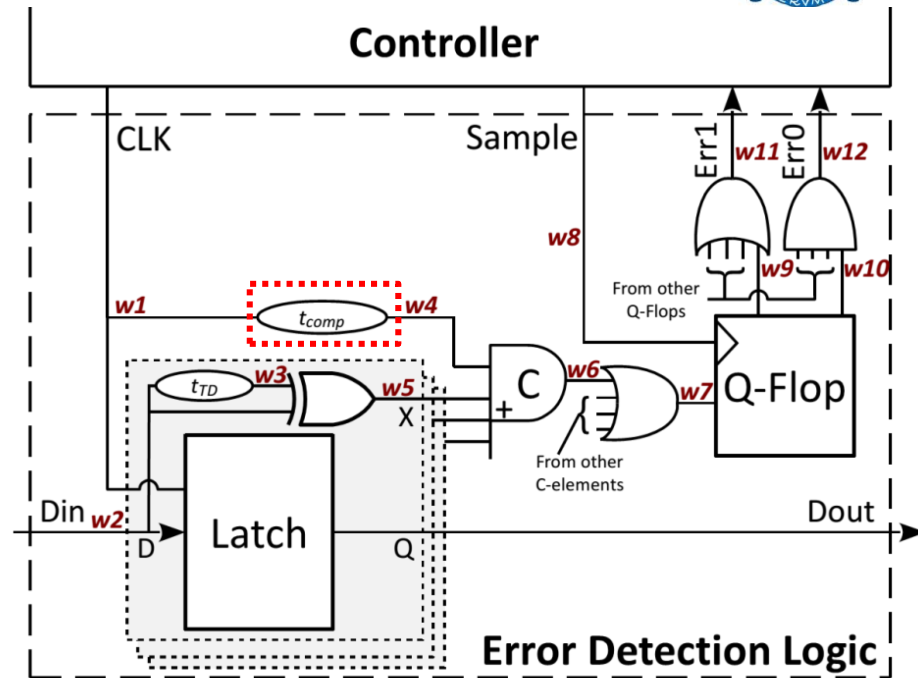

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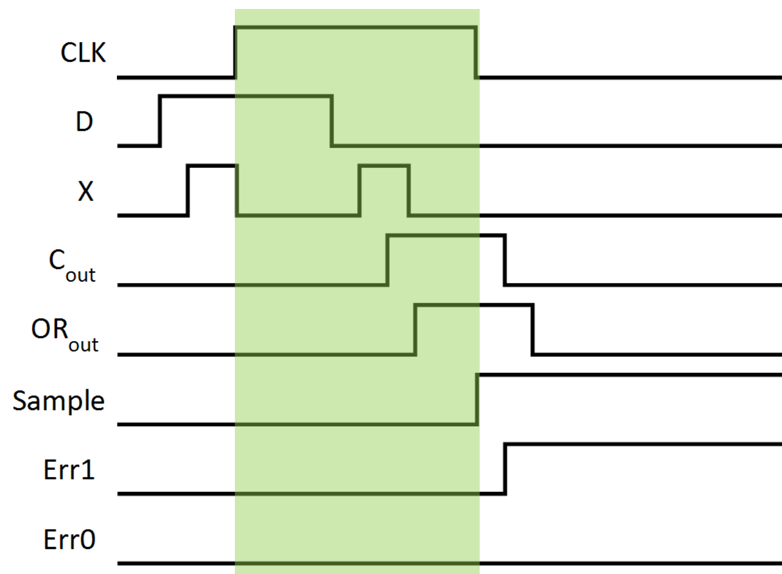

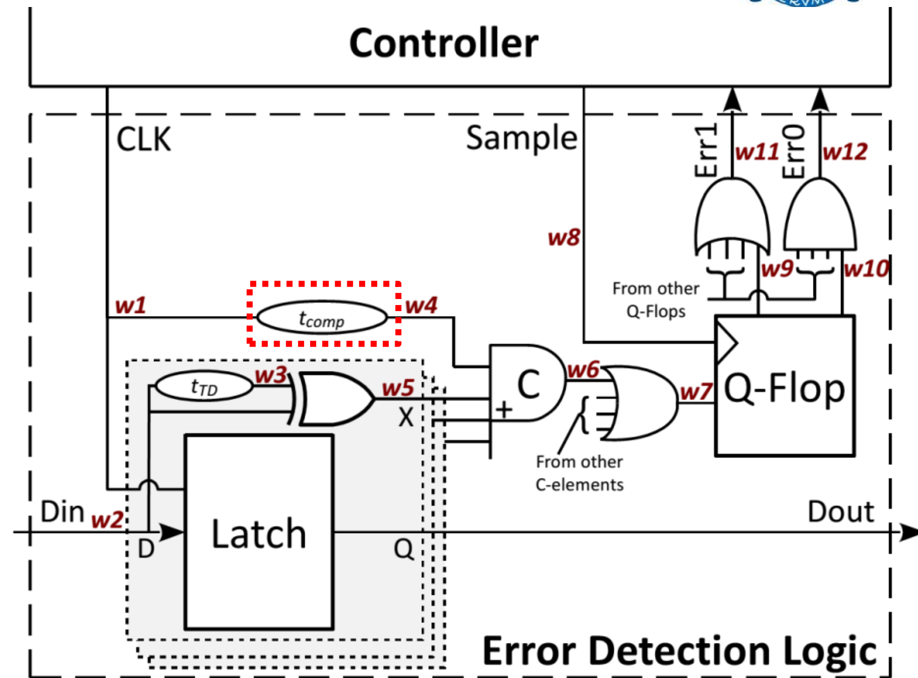

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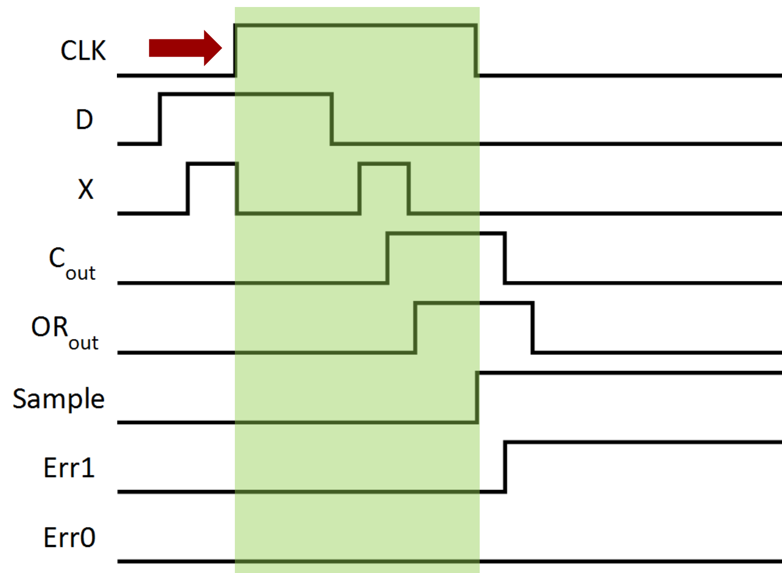

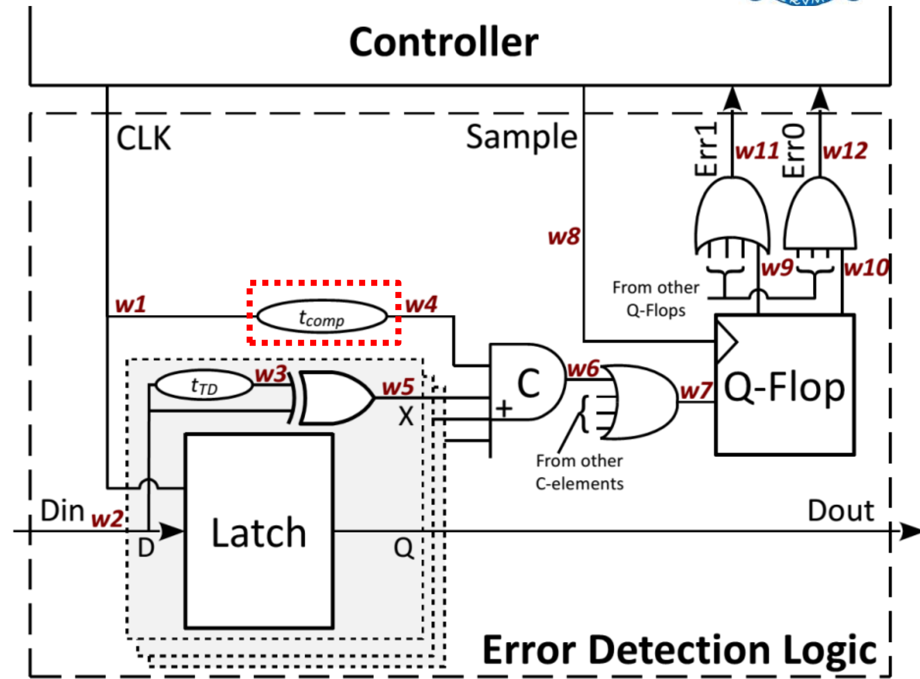

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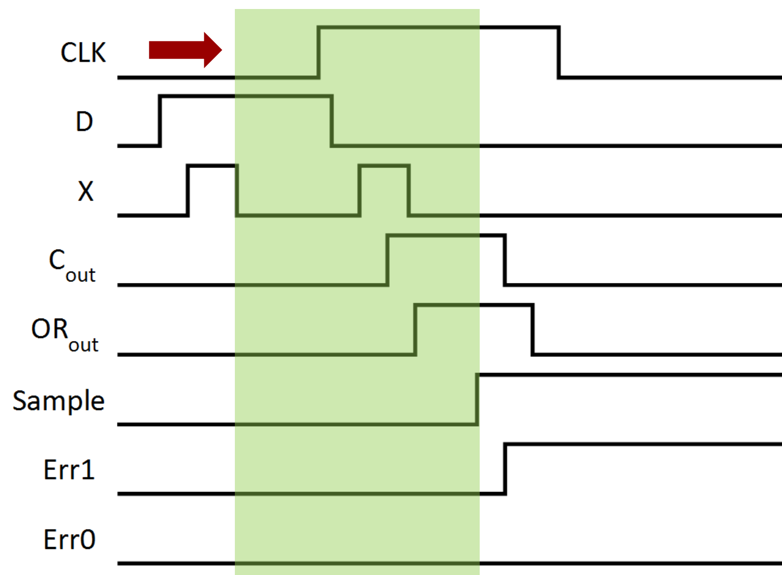

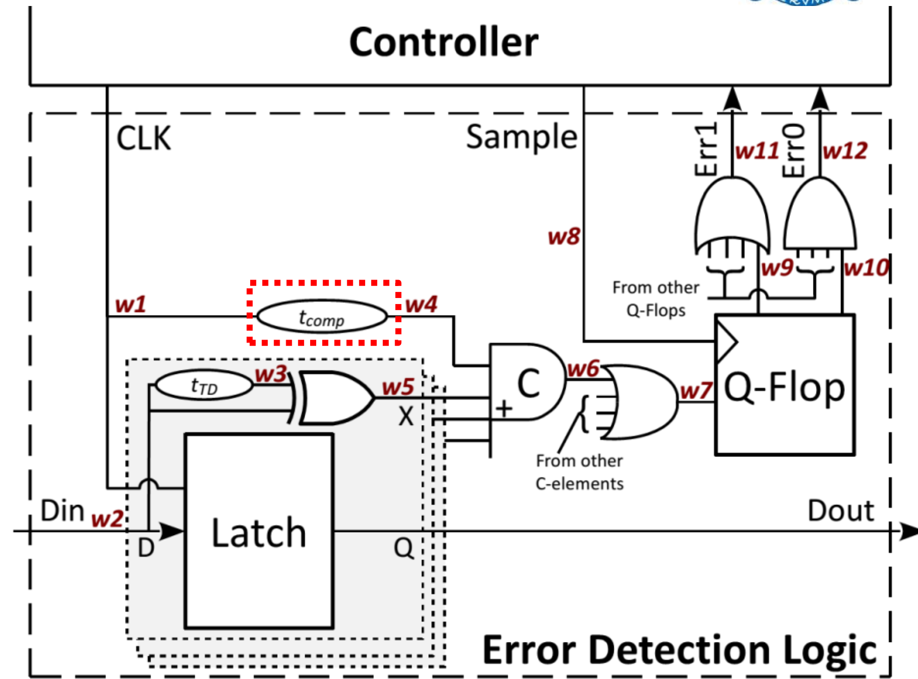

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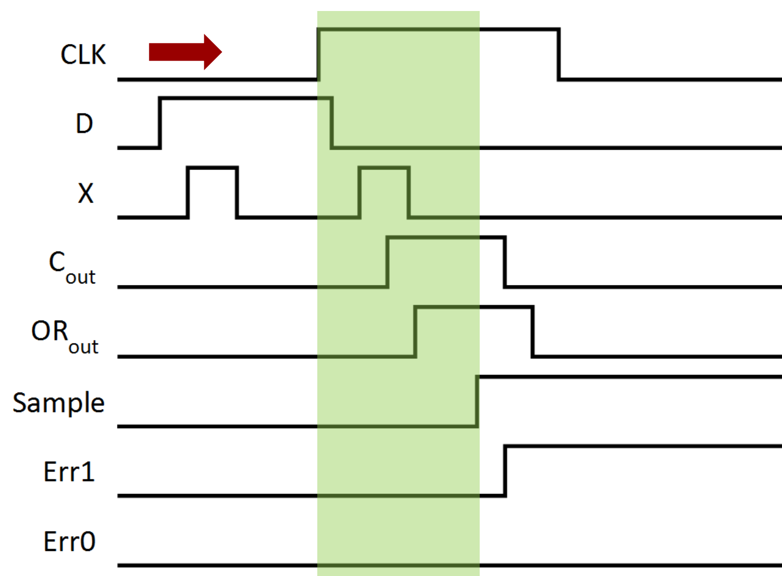

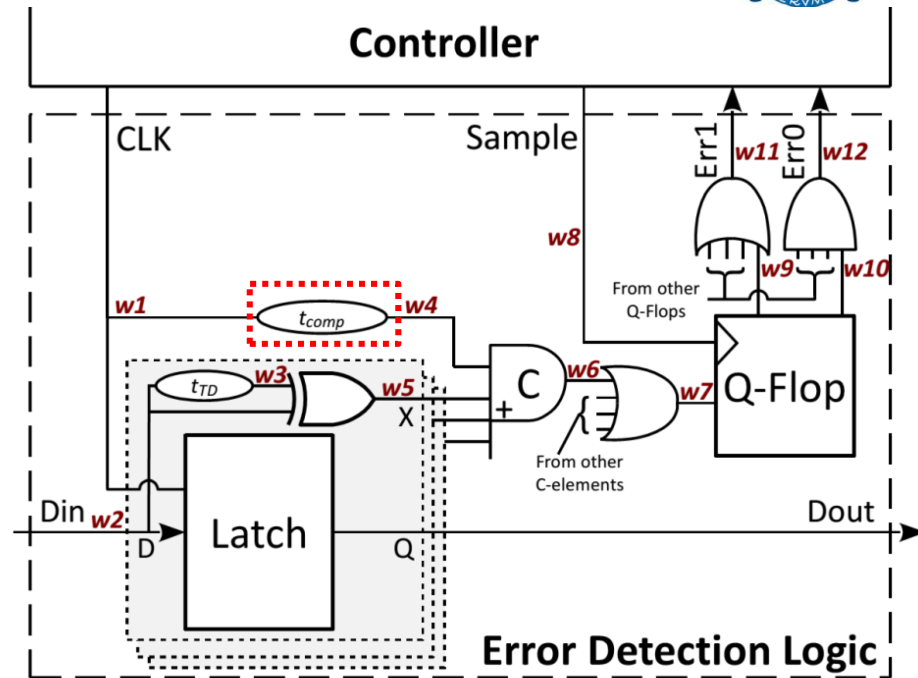

Delay Faults

- Delay line – t_{comp}
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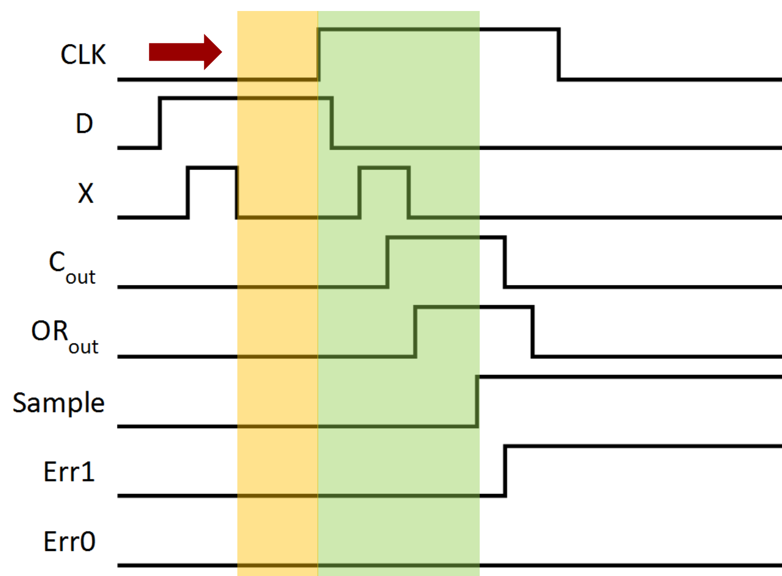
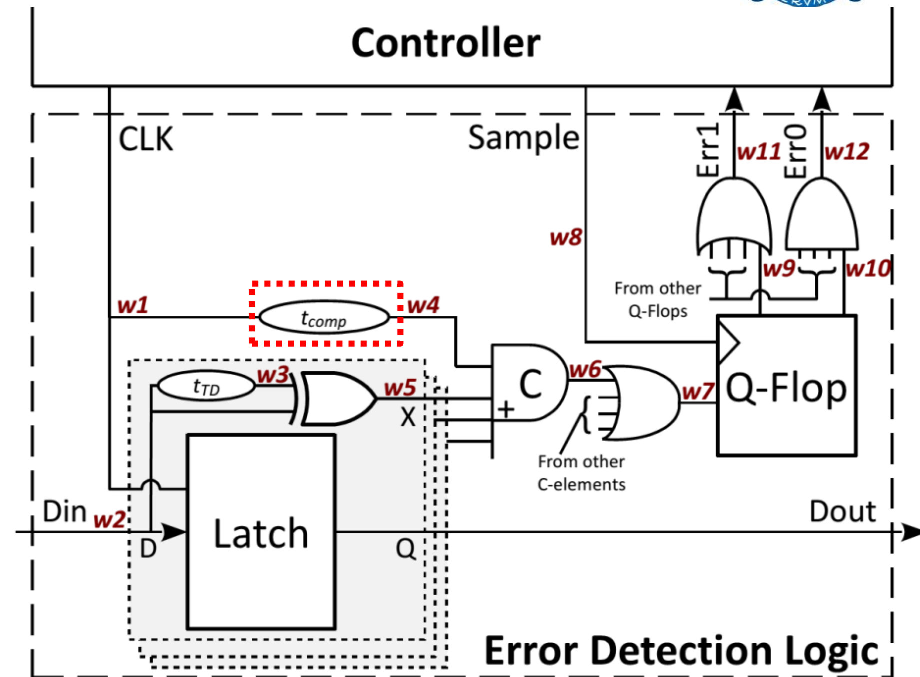
    - Undetectable without a TV
    - TV must be generated





TV at the beginning of TRW

Test Approaches

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Fault		Functional	Scan Chain	TV Gen.
Type	Wire/ Element			
SA0	$w1$	*	*	*
	$w2$	*	*	*
	$w3$		*	*
	$w4$			*
	$w5$			*
	$w6$			*
	$w7$			*
	$w8$	*	*	*
	$w9$			*
	$w10$	*	*	*
	$w11$			*
	$w12$	*	*	*

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Fault Type	Fault Wire/ Element	Functional	Scan Chain	TV Gen.
SA1	$w1$	*	*	*
	$w2$	*	*	*
	$w3$		*	*
	$w4$		*	*
	$w5$		*	*
	$w6$		*	*
	$w7$		*	*
	$w8$	*	*	*
	$w9$	*	*	*
	$w10$			*
	$w11$	*	*	*
	$w12$	*	*	*

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Fault		Functional	Scan Chain	TV Gen.
Type	Wire/ Element			
SPD	t_{comp}		*	*
	t_{TD}			*
LPD	*Latch*		*	*
	t_{comp}			*
	t_{TD}		*	*
	XOR Gate		*	*
	C-element			*
	OR Gate			*

Test Approaches

- Three approaches evaluated
  - Functional
  - Scan chain
    - Observability of Err1 and Err0
  - TV generator
    - Some faults are only observed when the circuit has a TV
    - Glitch generator
    - Delay test pattern

Fault Type	Fault Wire/ Element	Functional	Scan Chain	TV Gen.
SA0	$w1$	*	*	*
	$w2$	*	*	*
	$w3$		*	*
	$w4$			*
	$w5$			*
	$w6$			*
	$w7$			*
	$w8$	*	*	*
	$w9$			*
	$w10$	*	*	*
	$w11$			*
	$w12$	*	*	*
SA1	$w1$	*	*	*
	$w2$	*	*	*
	$w3$		*	*
	$w4$		*	*
	$w5$		*	*
	$w6$		*	*
	$w7$		*	*
	$w8$	*	*	*
	$w9$	*	*	*
	$w10$			*
	$w11$	*	*	*
	$w12$	*	*	*
SPD	t_{comp}		*	*
	t_{TD}			*
LPD	*Latch*		*	*
	t_{comp}			*
	t_{TD}		*	*
	XOR Gate		*	*
	C-element			*
	OR Gate			*
Coverage		34%	66%	100%

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	$w6$			*
	$w7$			*
	$w8$	*	*	*
	$w9$			*
	$w10$	*	*	*
	$w11$			*
	$w12$	*	*	*
SA1	$w1$	*	*	*
	$w2$	*	*	*
	$w3$		*	*
	$w4$		*	*
	$w5$		*	*
	$w6$		*	*
	$w7$		*	*
	$w8$	*	*	*
	$w9$	*	*	*
	$w10$			*
	$w11$	*	*	*
	$w12$	*	*	*
SPD	t_{comp}		*	*
	t_{TD}			*
LPD	*Latch*		*	*
	t_{comp}			*
	t_{TD}		*	*
	XOR Gate		*	*
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  - Investigate alternatives for TV generation
  - Apply this fault analysis and classification to other resilient designs

Questions?