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The Metastable Behavior of a Schmitt-Trigger

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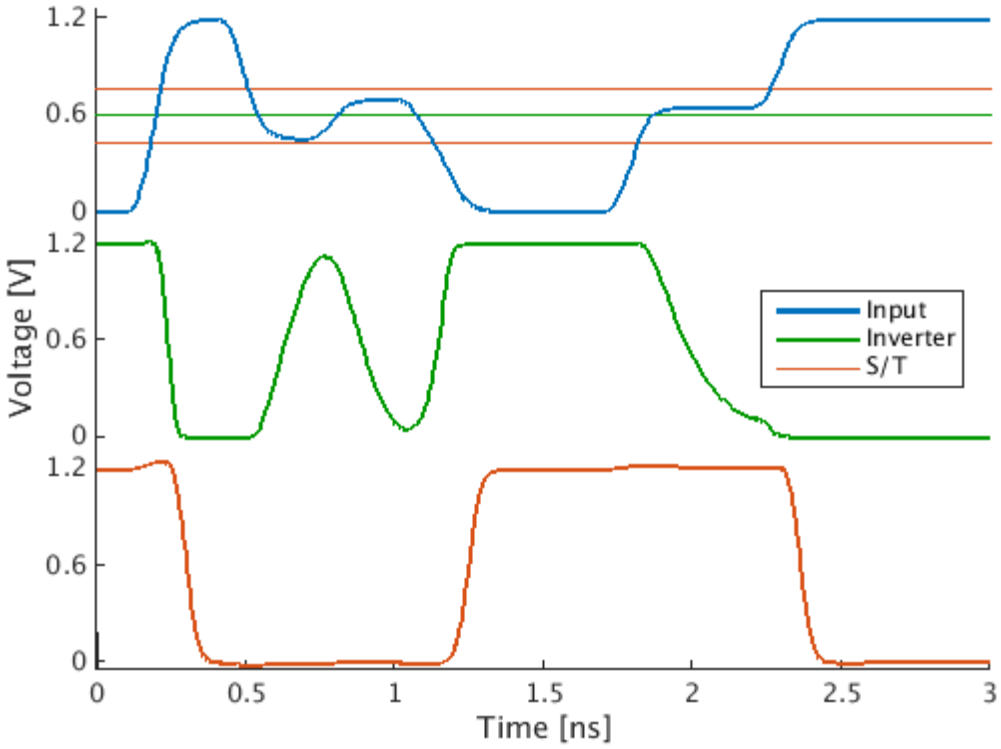
Outline

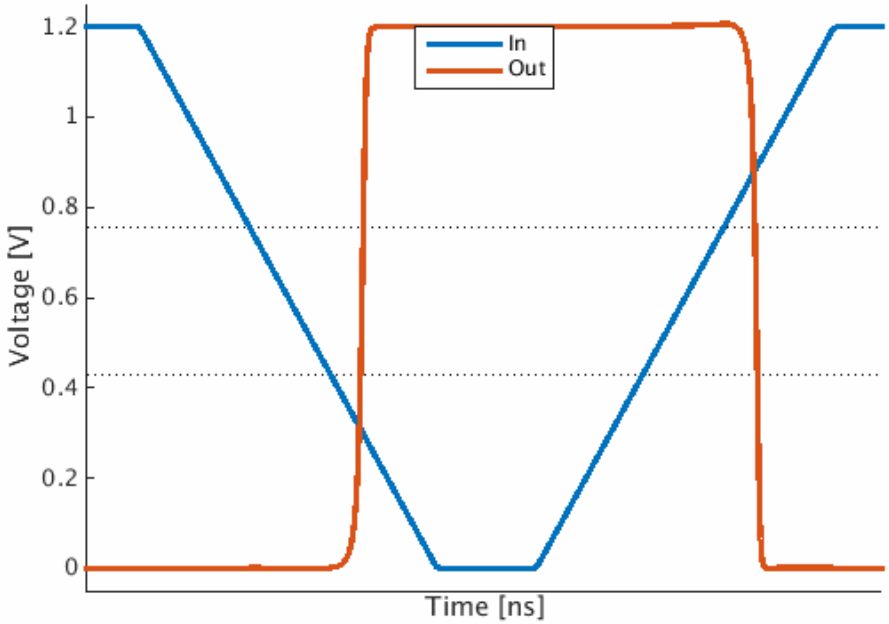
- What is a Schmitt-Trigger?
- Metastable or not?
- Marino's model
- Analysis of typical scenarios
- The promised answers
- Conclusion & future work

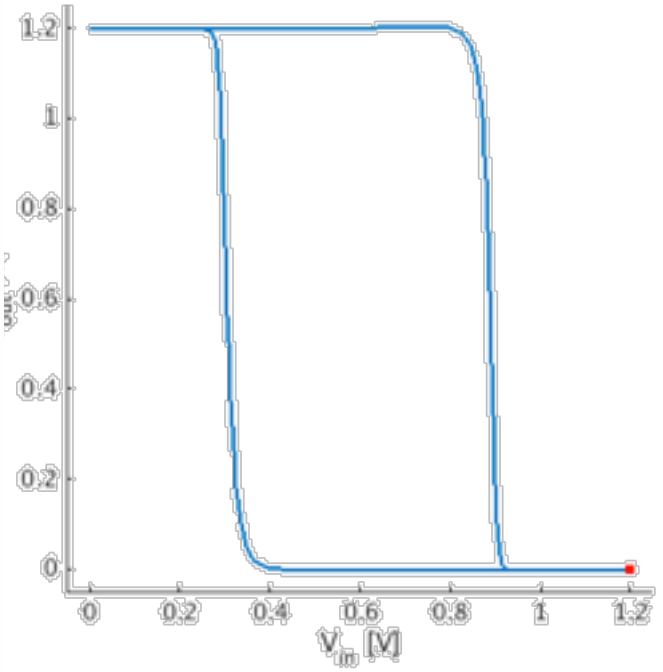
Why a Schmitt-Trigger?

To turn unclean signals into well-behaved ones appropriate for digital processing



Schmitt-Trigger Operation

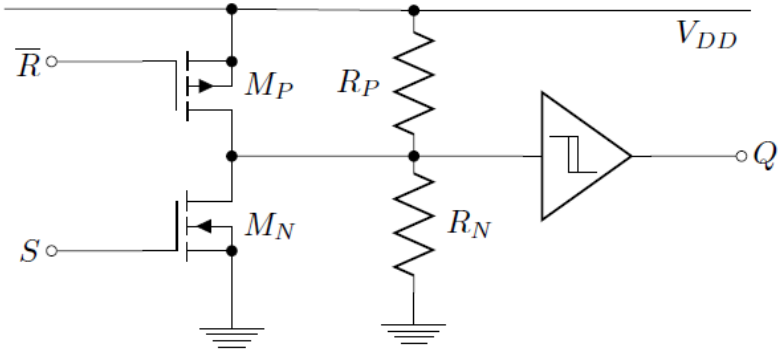


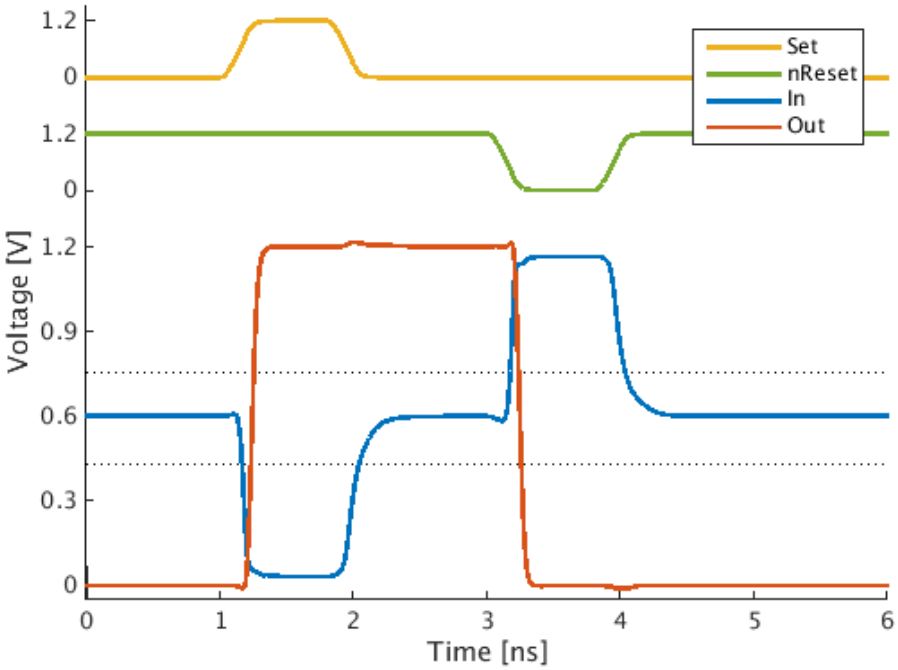


Hysteresis is attained by making the input threshold depend on current output

Can a Schmitt-Trigger be Metastable?

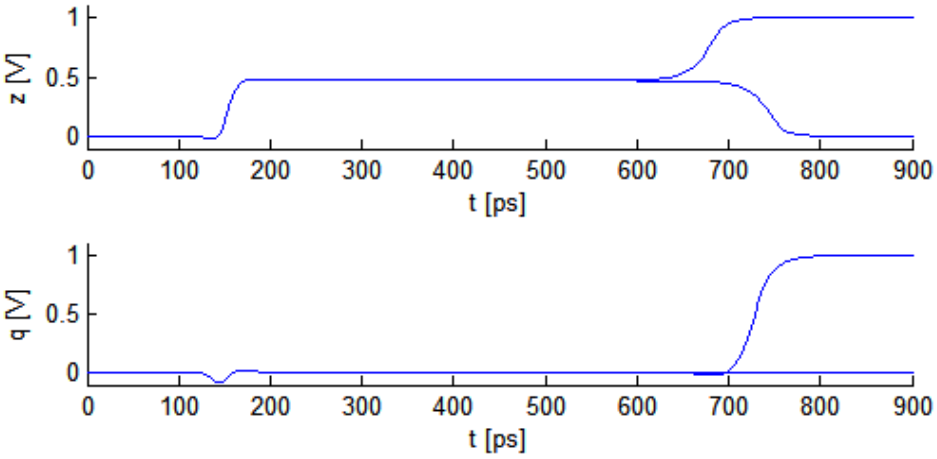
- It is “just an inverter with two thresholds”…
- BUT: It must have feedback from the output
- Can this be the perfect RS-latch?





Can this circuit actually work?

- *Metastability filter for Muller C-element*
- Where is the gain if the Schmitt-Trigger gets metastable itself?

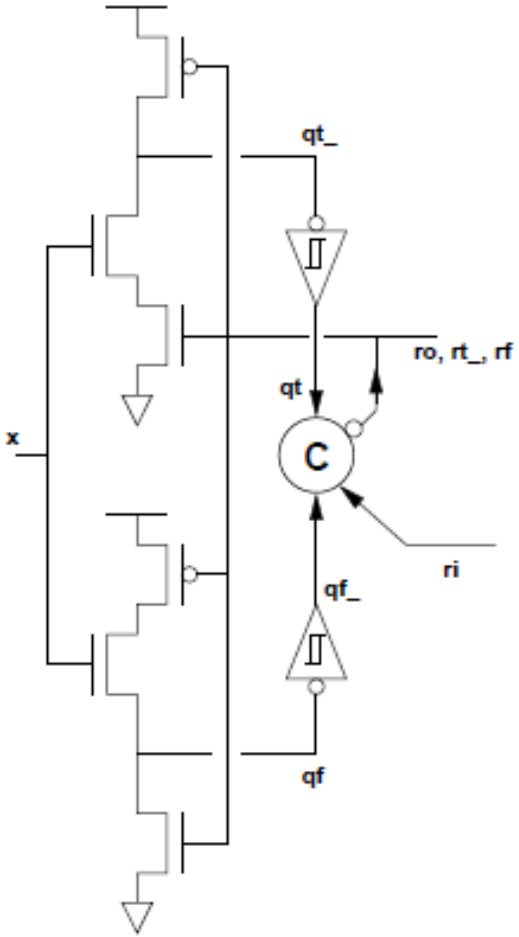


[Polzer, Steininger, Lechner: Muller C-Element Metastability Containment, 2013]

Does this circuit work safely?

- A *clock-handshake interface*
- Integrators produce monotonic waveform
- “The outputs of the integrators have been augmented with Schmitt-trigger inverters to guarantee quick transitions…”

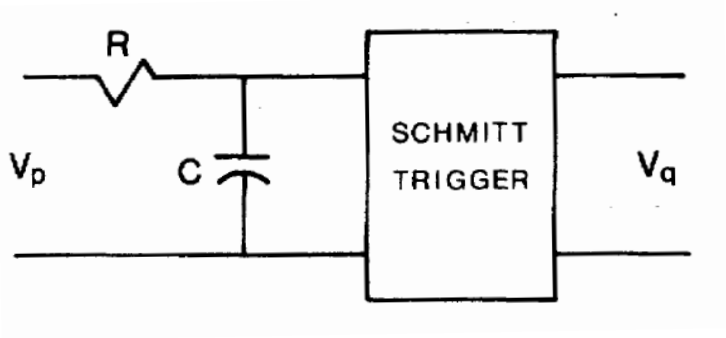
⇨ What about S/T metastability?



[Martin, Nyström: Asynchronous techniques for system-on-chip design, 2006]

What about input filtering?

- *Huffman's Inertial Delay Element*
- Low pass at S/T input to prevent metastability
- Perfect ID allows building a perfect synchronizer
- Can this ID implementation be perfect?

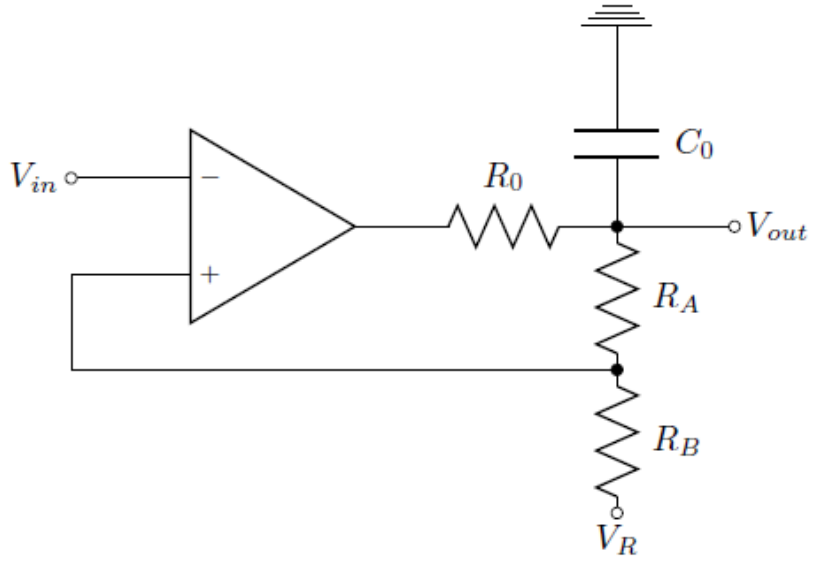


- This is analyzed in Marino's paper

[Marino: The Effect of Asynchronous Inputs on Sequential Network Reliability, 1977]

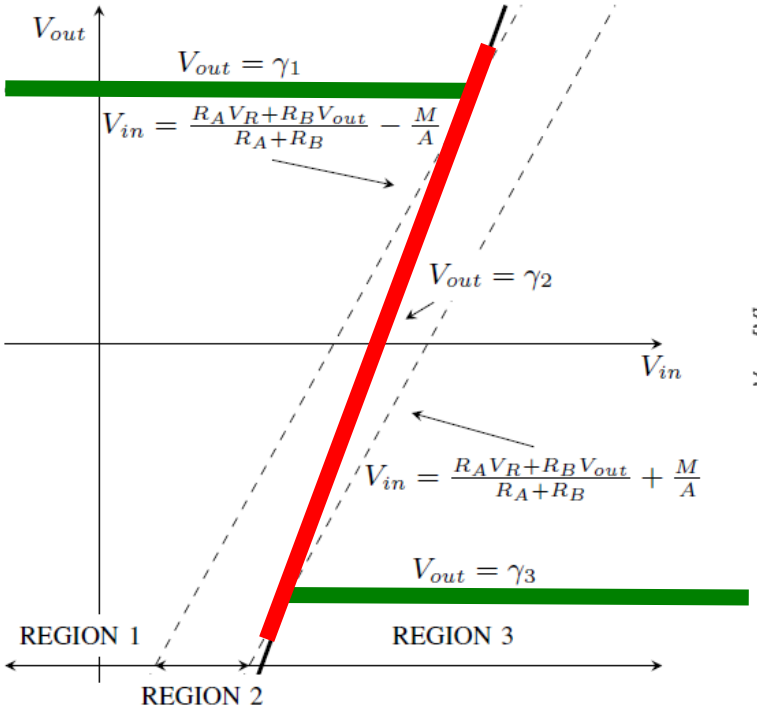
Marino‘s Model

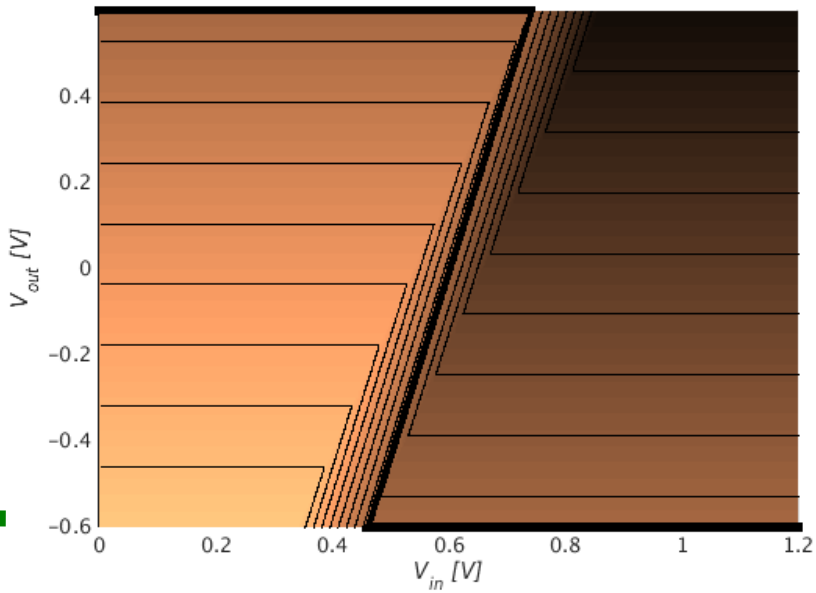
- Based on ideal op-amp with positive feedback
- First order low pass to limit output dynamics



Marino‘s Model

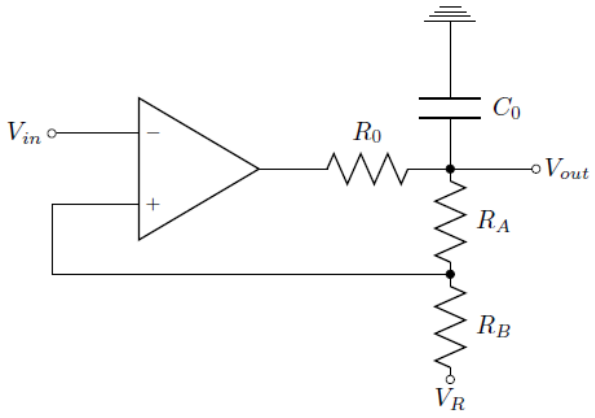
- Phase plane shows (meta-) stable state
- Equations for derivative of output w.r.t. time

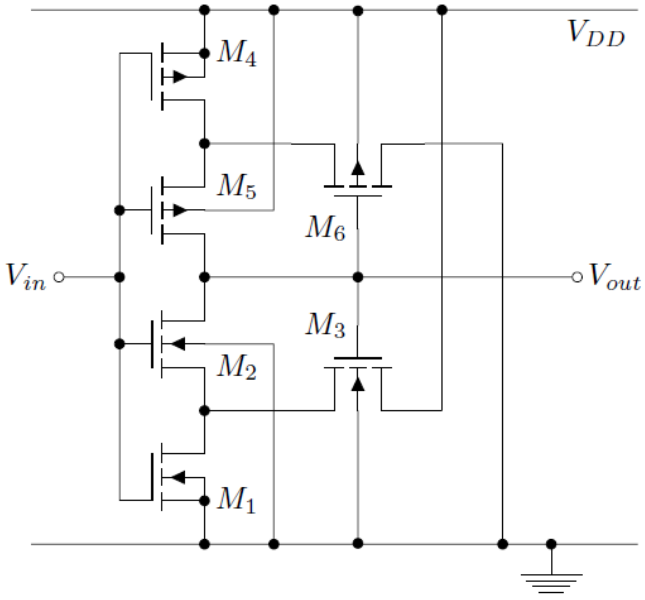




Realistic Implementations

- We used realistic op-amp models in HSPICE simulations
  - Commercial op-amp model (EL5165)
  - CMOS implementation (With 65 nm library)

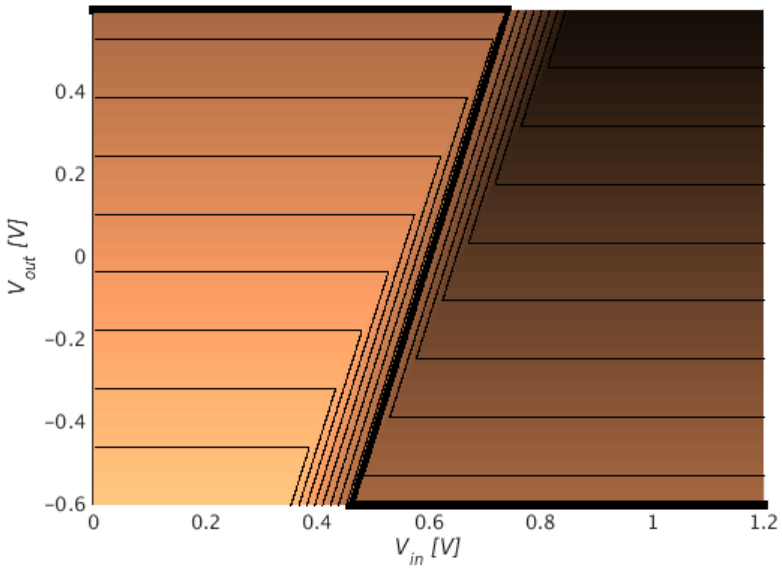




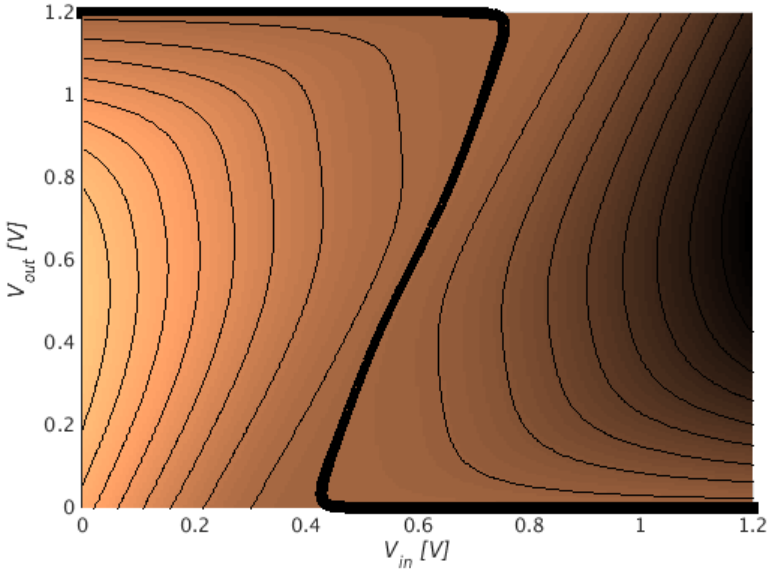
Model vs. Simulation

- They differ in quantitative details but give the same qualitative results

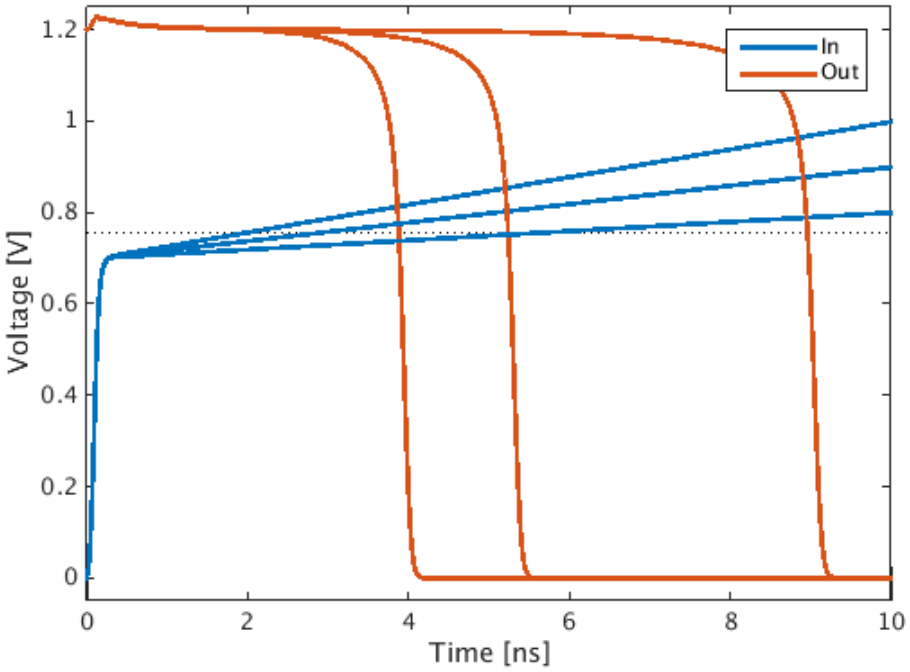
Model

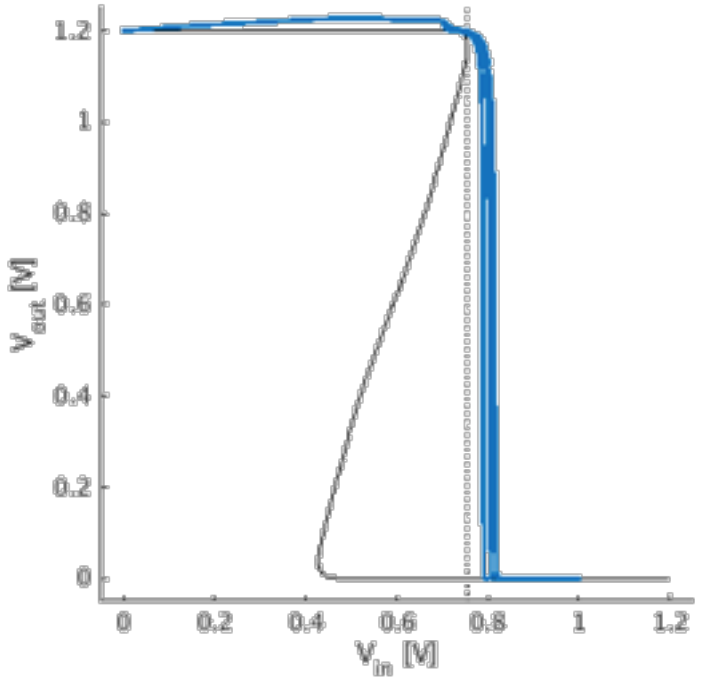


Simulation



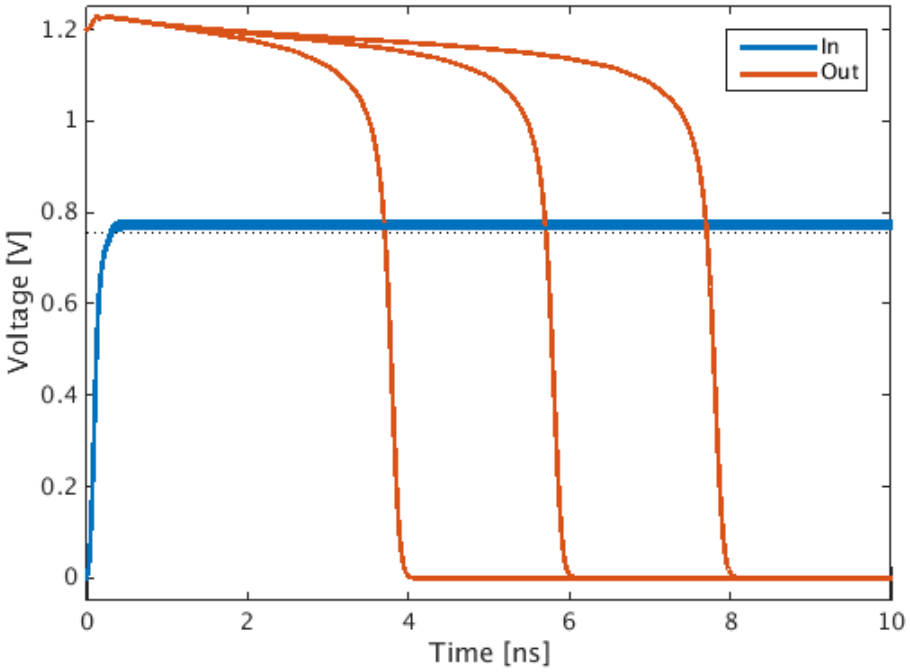
Strictly Monotonic Inputs

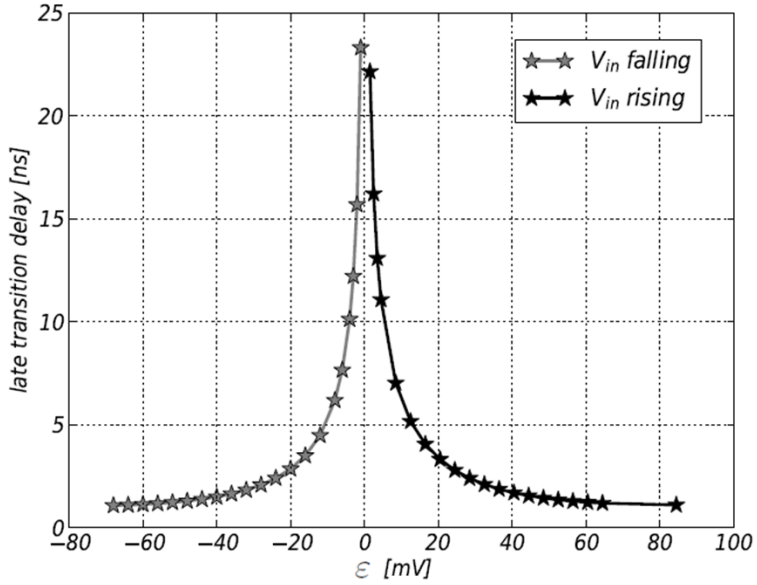




Once tripped, trajectory cannot move back to a metastable state ⇨ clean transitions

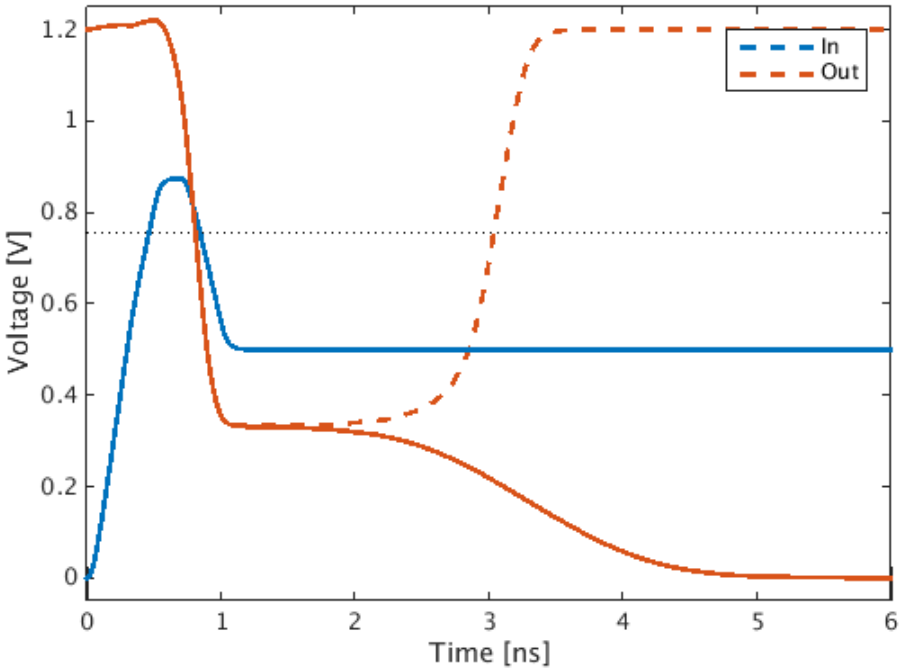
Monotonic Input Trace Staying Constant

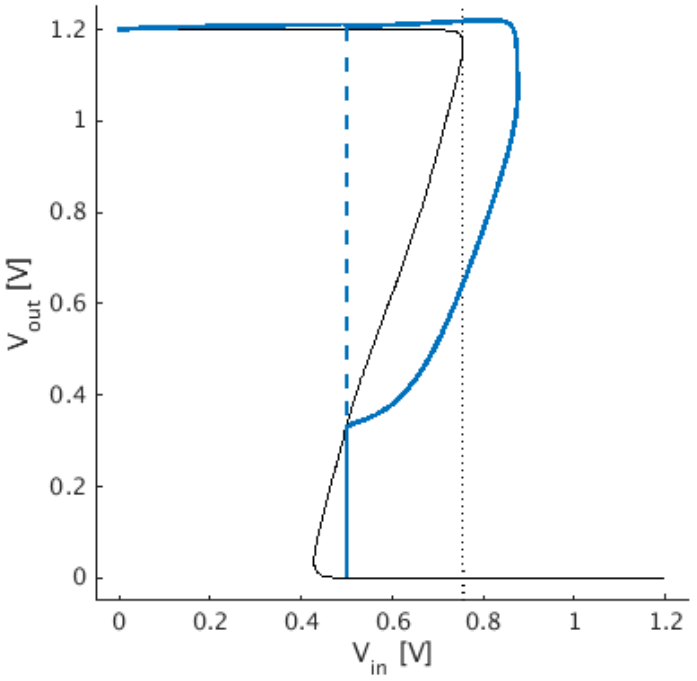




Can stay indefinitely long on tripping point, *i.e.* metastable with clear HI at output ⇨ late transition

Producing Intermediate Output



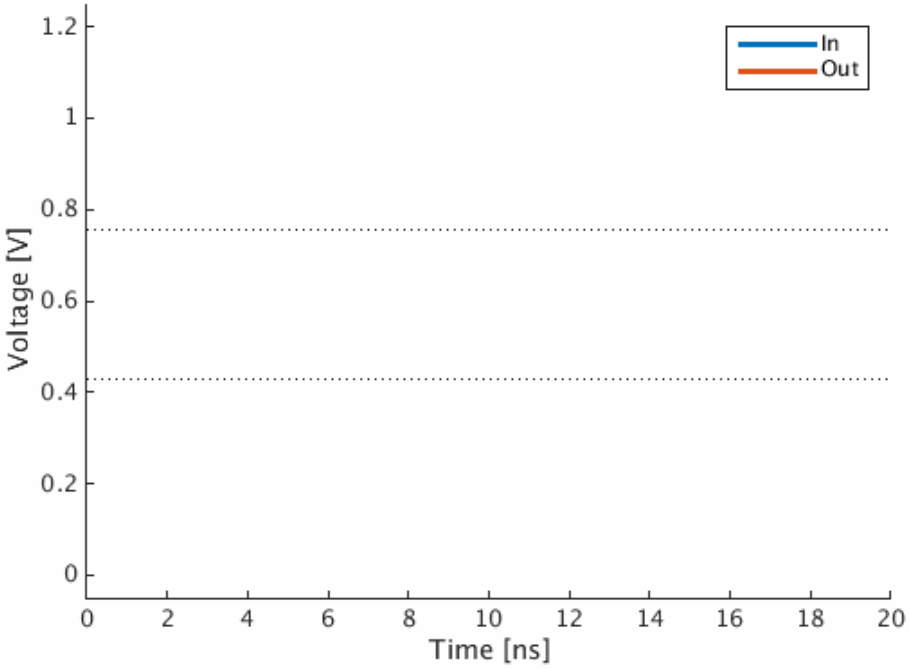


With an appropriate input, the S/T can be made metastable

⇨ "constant" output depending on input; resolving to HI/LO

☝ Not what we know from latch et al.

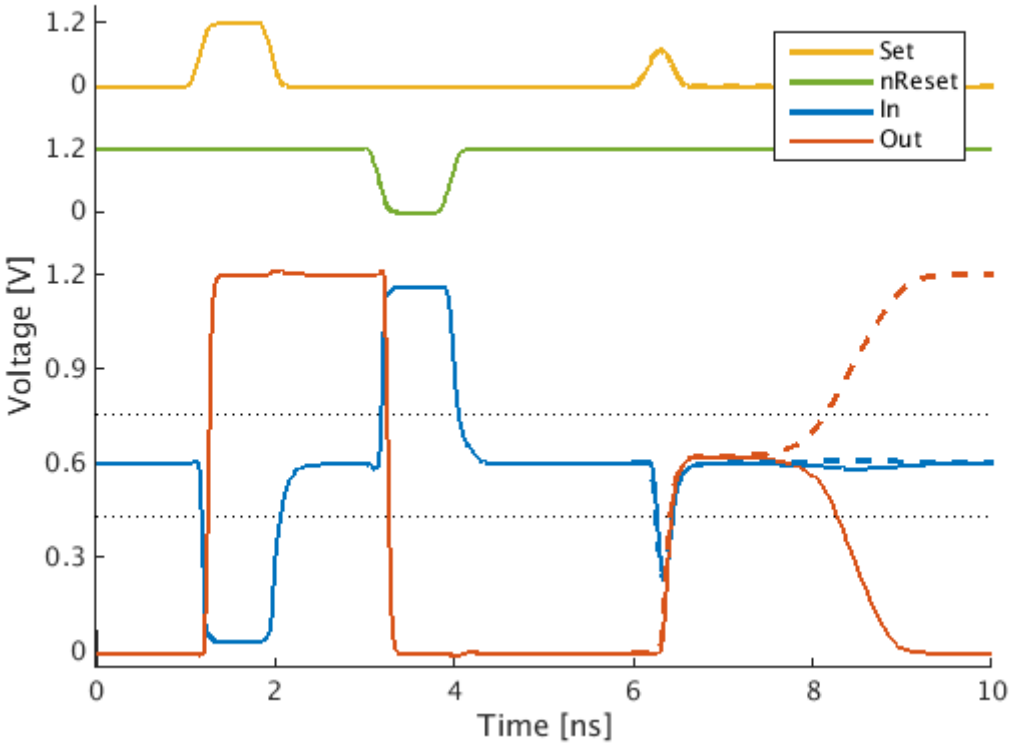
Producing Arbitrary Output



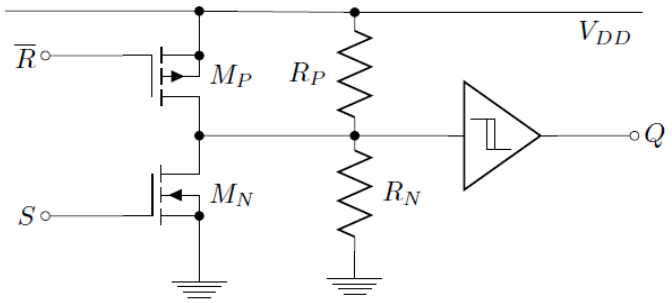
Moving input while S/T resolves moves metastable voltage

⇨ arbitrary waveforms while metastable

Perfect Latch Revisited

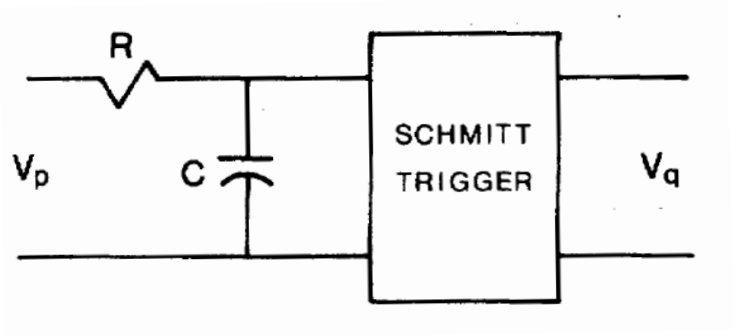


There is no perfect latch!

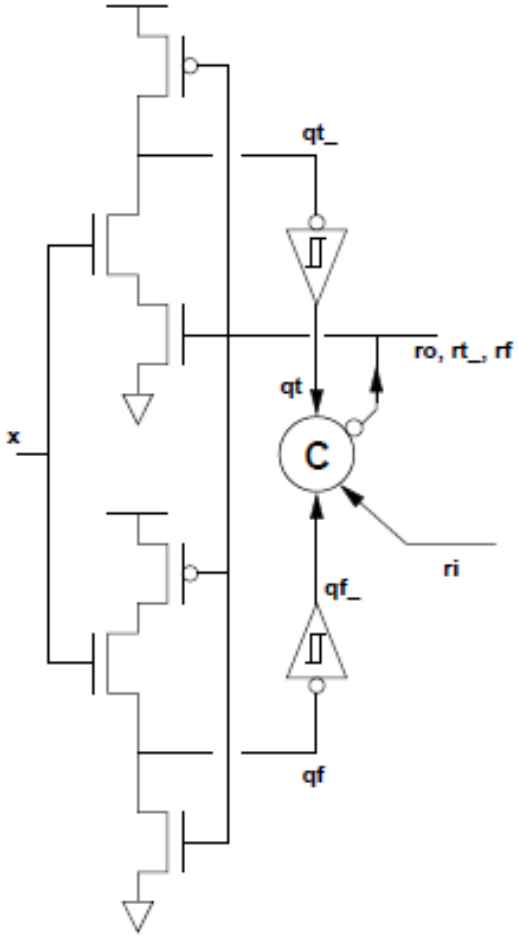


The other circuits

Works safely – monotonic input once C-element resolves



Not safe!

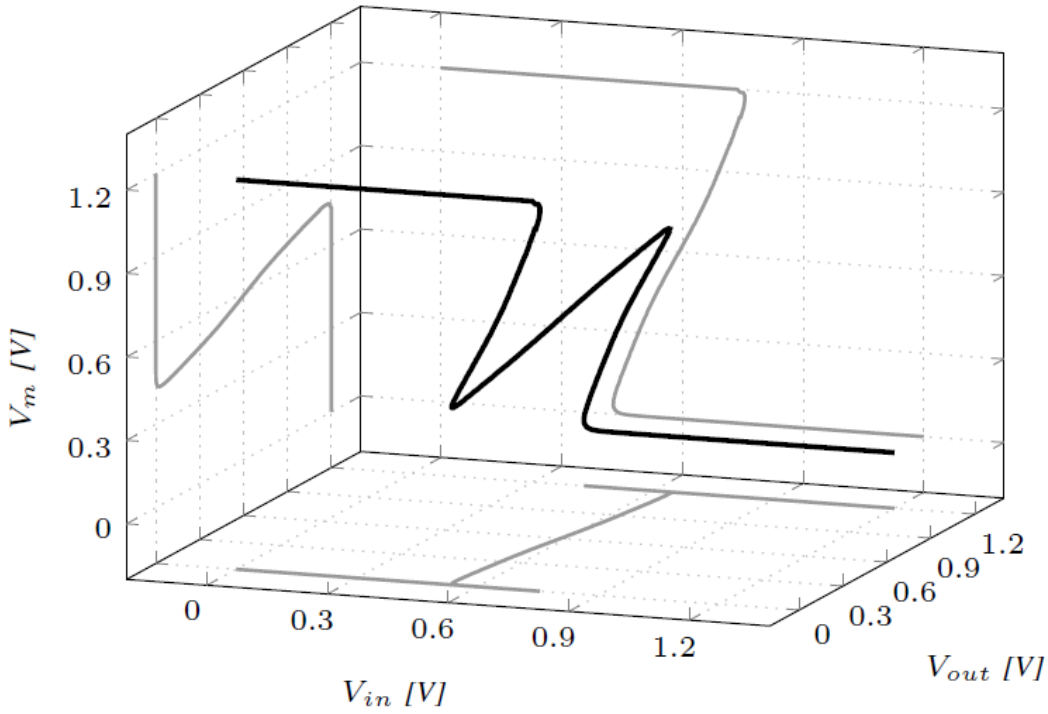


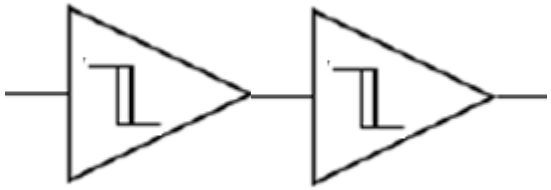
Safe but late transitions possible

Conclusions

- S/T may become metastable
- Output voltage may have any value when metastable
- strictly monotonic input ⇨ clean transition
- constant input at tripping point ⇨ late transition
- non-monotonic input ⇨ any waveform possible

Future Work: S/T Cascade





Needs three dimensions for the characteristic

Conclusions

- S/T may become metastable
- Output voltage may have any value when metastable
- Strictly monotonic input ⇨ clean transition
- Constant input at tripping point ⇨ late transition
- Non-monotonic input ⇨ any waveform possible

Thank you!