Impact of Process Variations on Synchronizer Performance: An Experimental Study

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May 9, 2016

Outline of Presentation

- Metastability problem and effect of variations
- Background study
- Experimental study on FPGA
- Observations
- Summary

Metastability and MTBF

- Metastability
  - Clock domain crossing
  - Asynchronous input to flip-flops
  - Long delays in interconnects
- Mean time between failure (MTBF)

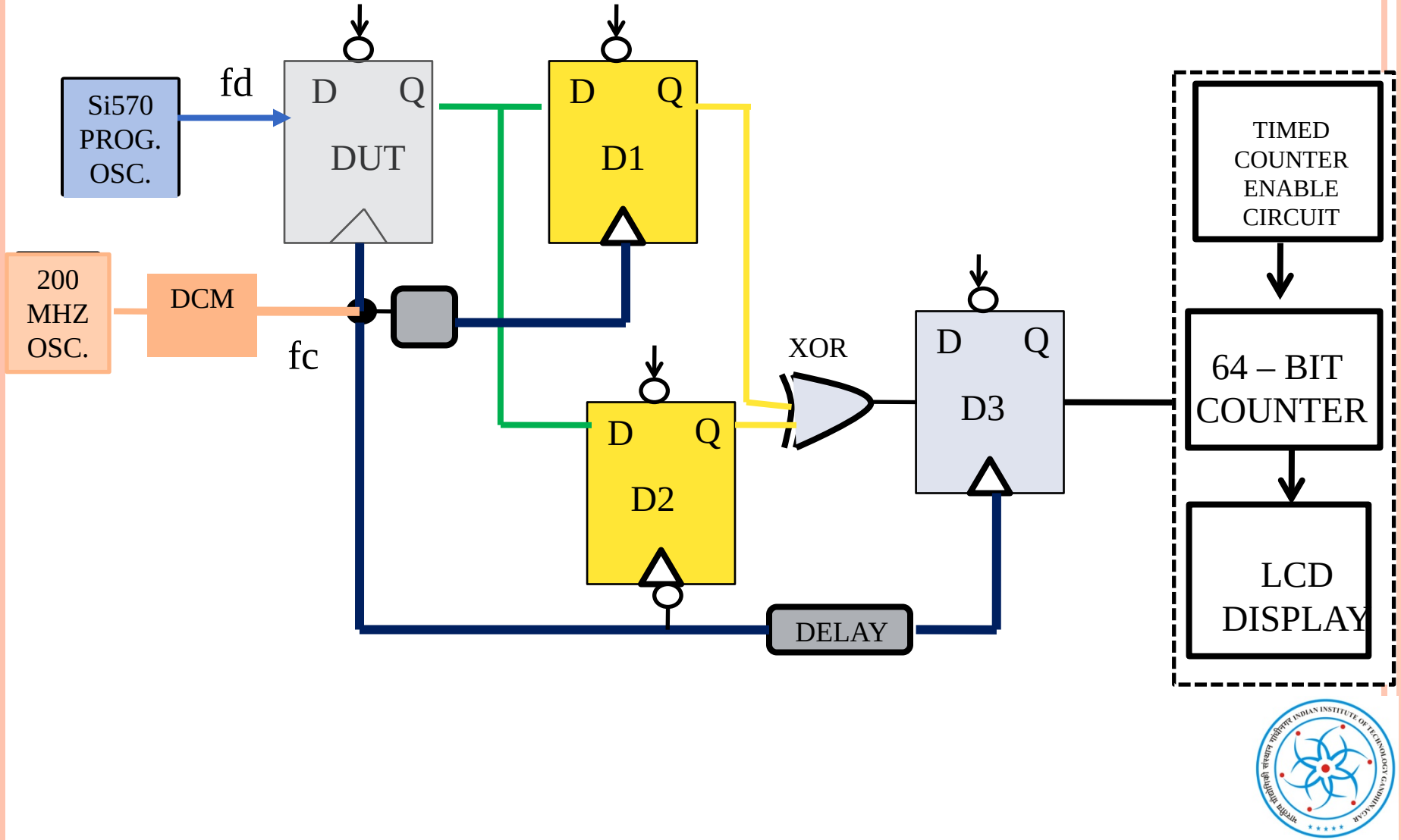
$$MTBF = \frac{e^{t_a/\tau}}{T_\omega \cdot f_C \cdot f_d}$$

- Process, Supply-voltage, Temperature variations affect τ and MTBF

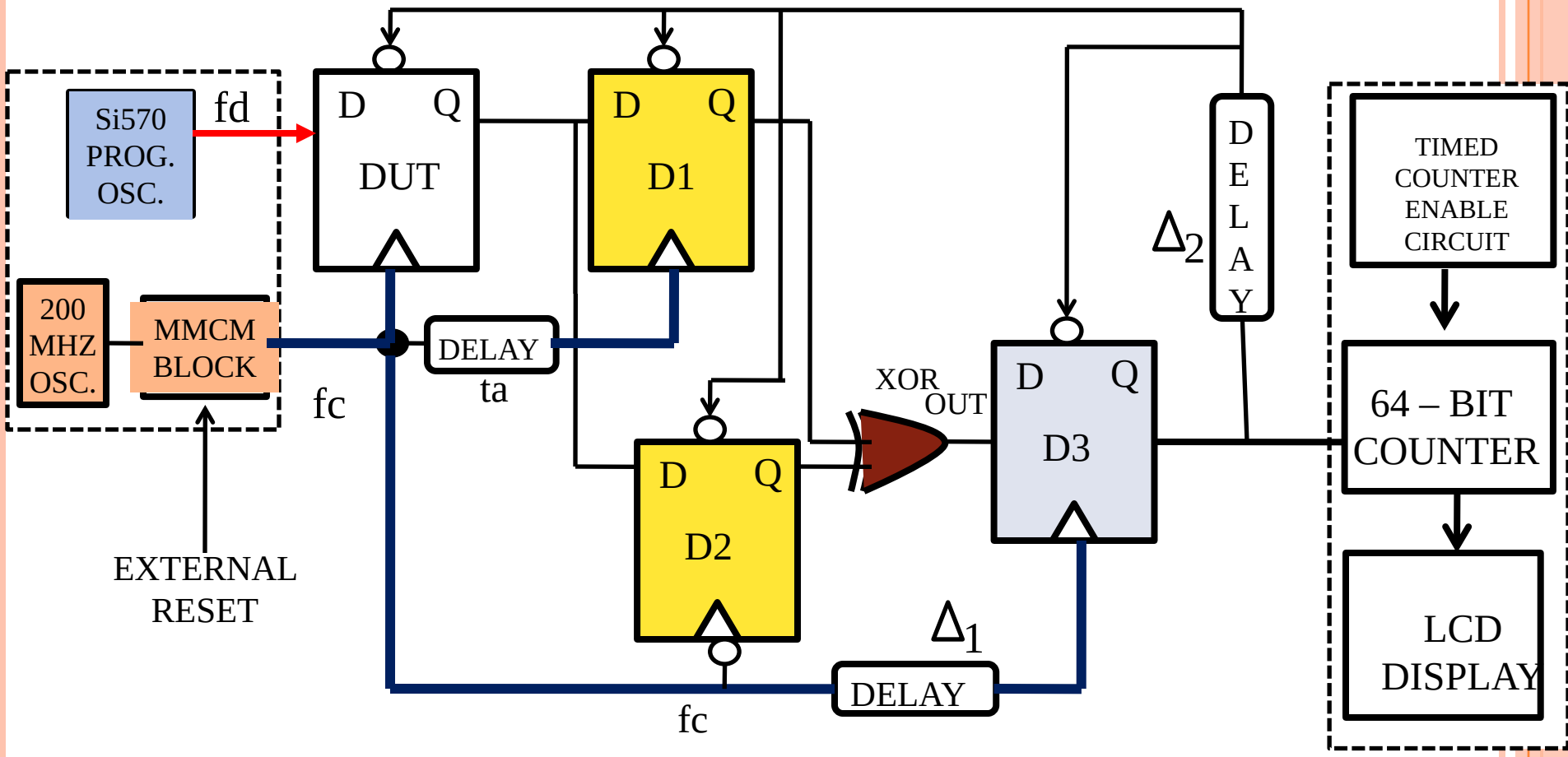
Metastability measurements: Prior work

- Metastability measurements
  - Polzer *et al*, Metastability characterization on FPGA [2013]
  - Rogina *et al*, Metastability testing on FPGA [2010]
  - S. Beer *et al*, Devolution of Synchronizer [2010]
  - Zhou *et al*, Deep metastability [2008]
- Variations study on Metastability
  - S. Beer *et al*, Effect of supply voltage and temperature variations on MTBF [2015]

Experimental Setup for MTBF measurements on FPGA



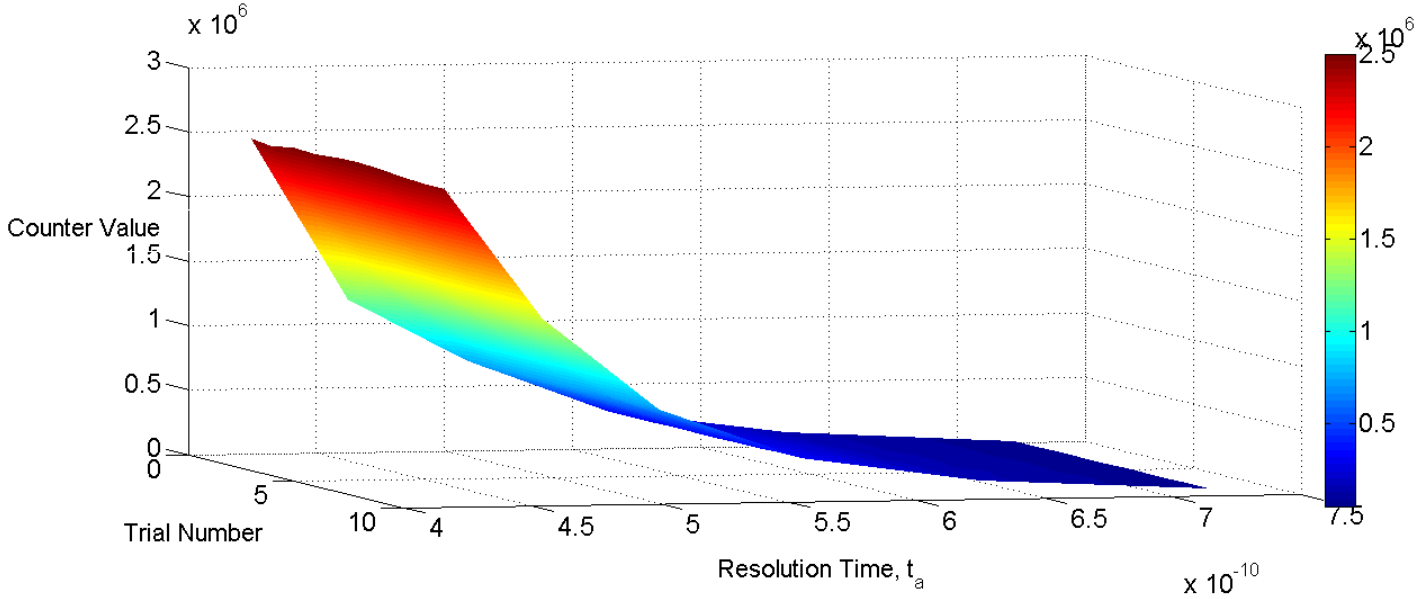
Experimental Setup for MTBF measurements on FPGA



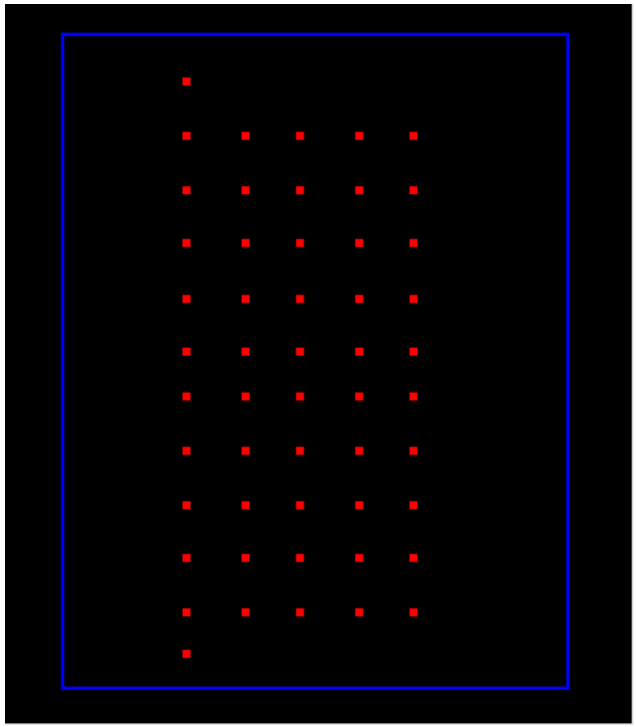
TAU CALCULATIONS

$$MTBF = \frac{counter - enable - time}{average\ counter\ value, n}$$

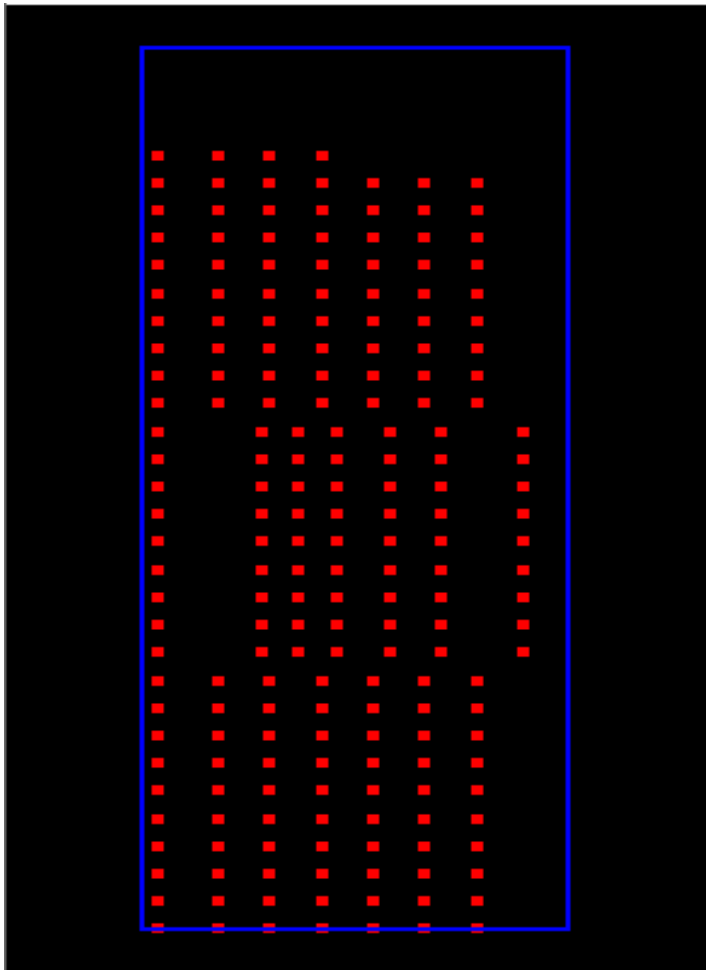
$$MTBF = \frac{e^{t_a/\tau}}{T_\omega \cdot f_C \cdot f_d}$$



Experiments for WID / D2D variations

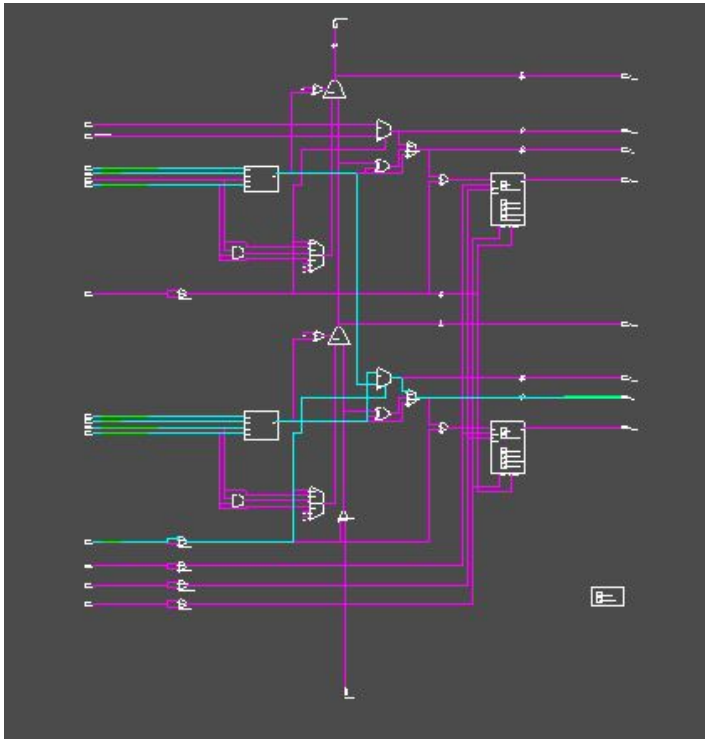


Spartan 3E (90 nm)

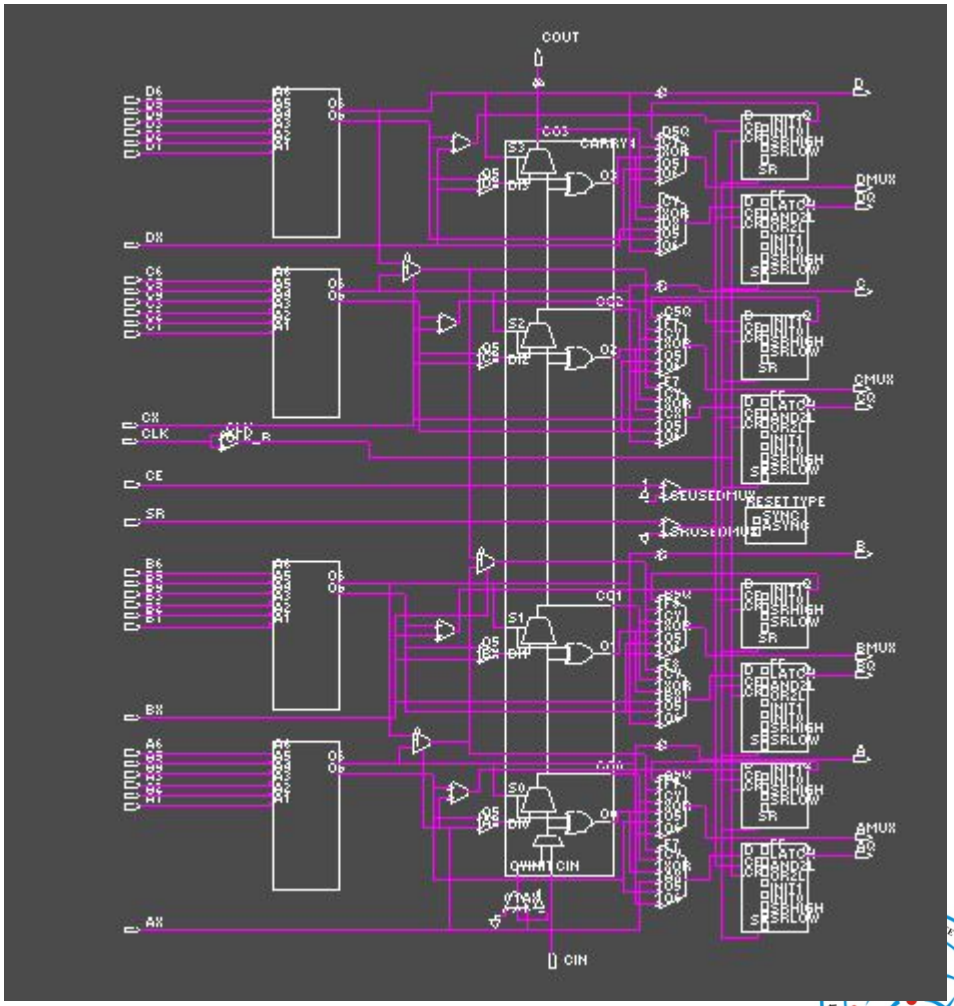


Kintex 7 (28nm)

Slice arrangement in FPGAs

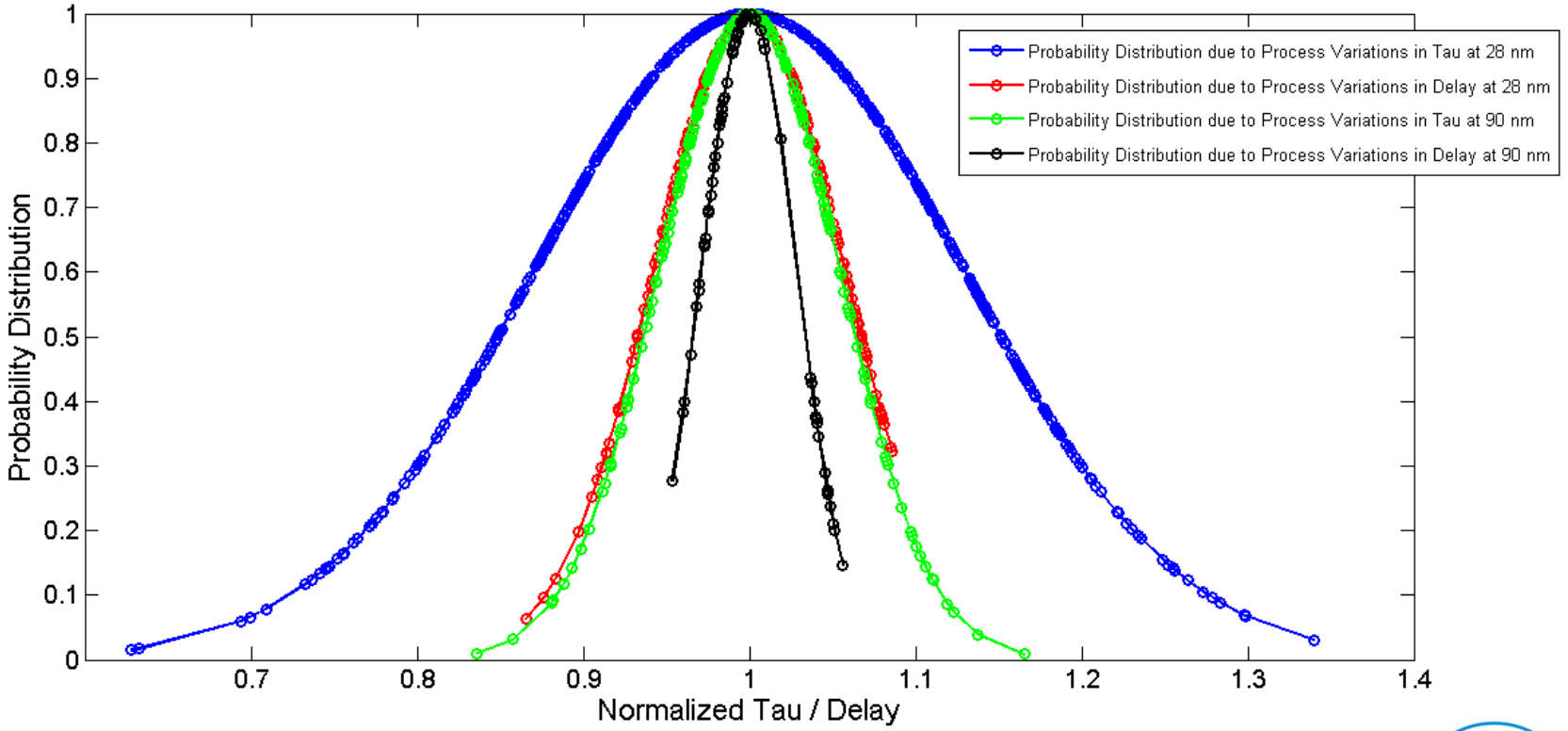


Spartan 3E (90 nm)



Kintex 7 (28nm)

Normalized TAU and DELAY Plots



SUMMARY

- Metastability characterization in Flip-flops used in FPGA boards
- Experiments on Spartan (90nm) and Kintex (28nm) boards
- Attempt to study Within-Die and Die-to-Die variations using FPGA setup
- Results show larger variation in τ for Kintex (28nm) board than for Spartan (90 nm) board across boards and across different locations
- Other factors – temperature, supply voltage, noise, etc. not addressed in this study

THANK YOU