Comparative Study of Synchronizer Circuits

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Outline of Presentation

- Synchronizer Circuits
- Analysis of three synchronizer circuits using small-signal modeling
- Comparison with simulations
- Comparison with experimental data
- Summary and conclusions

OBJECTIVE OF THIS WORK

- Mean time between failure (MTBF)

Synchronizer circuit

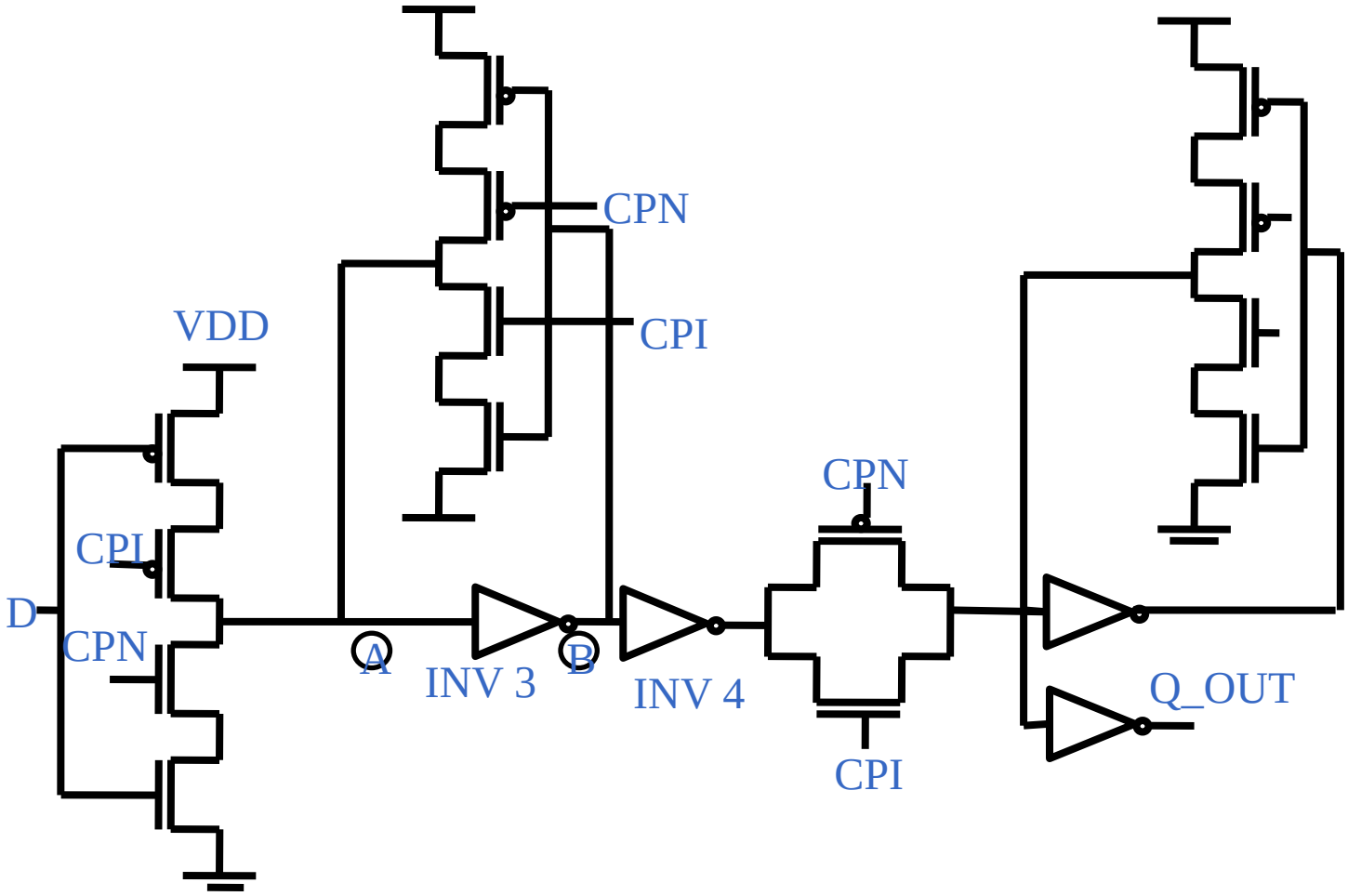
Technology scaling

$$MTBF = \frac{e^{t_a/\tau}}{T_\omega \cdot f_C \cdot f_d}$$

PVT Variations

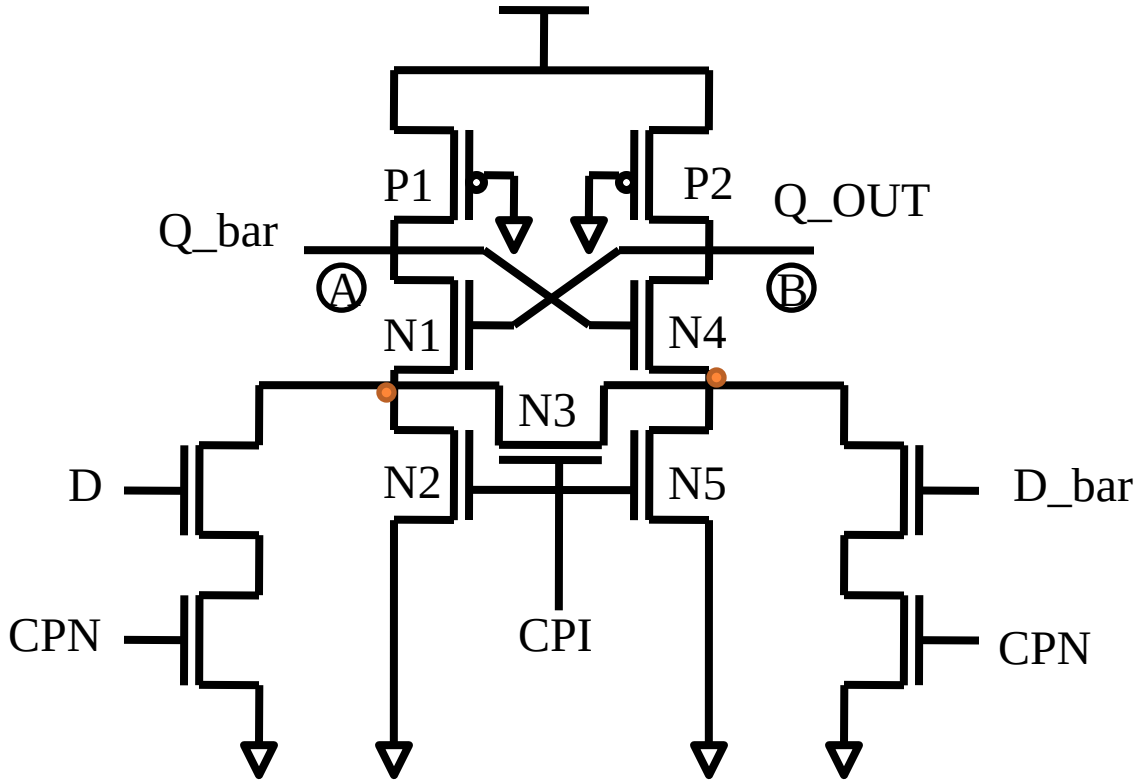
Effect of synchronizer circuit design, technology scaling and process variations in τ and MTBF: Analysis, Simulations, Experiments

SYNCHRONIZER CIRCUITS : STANDARD DFF



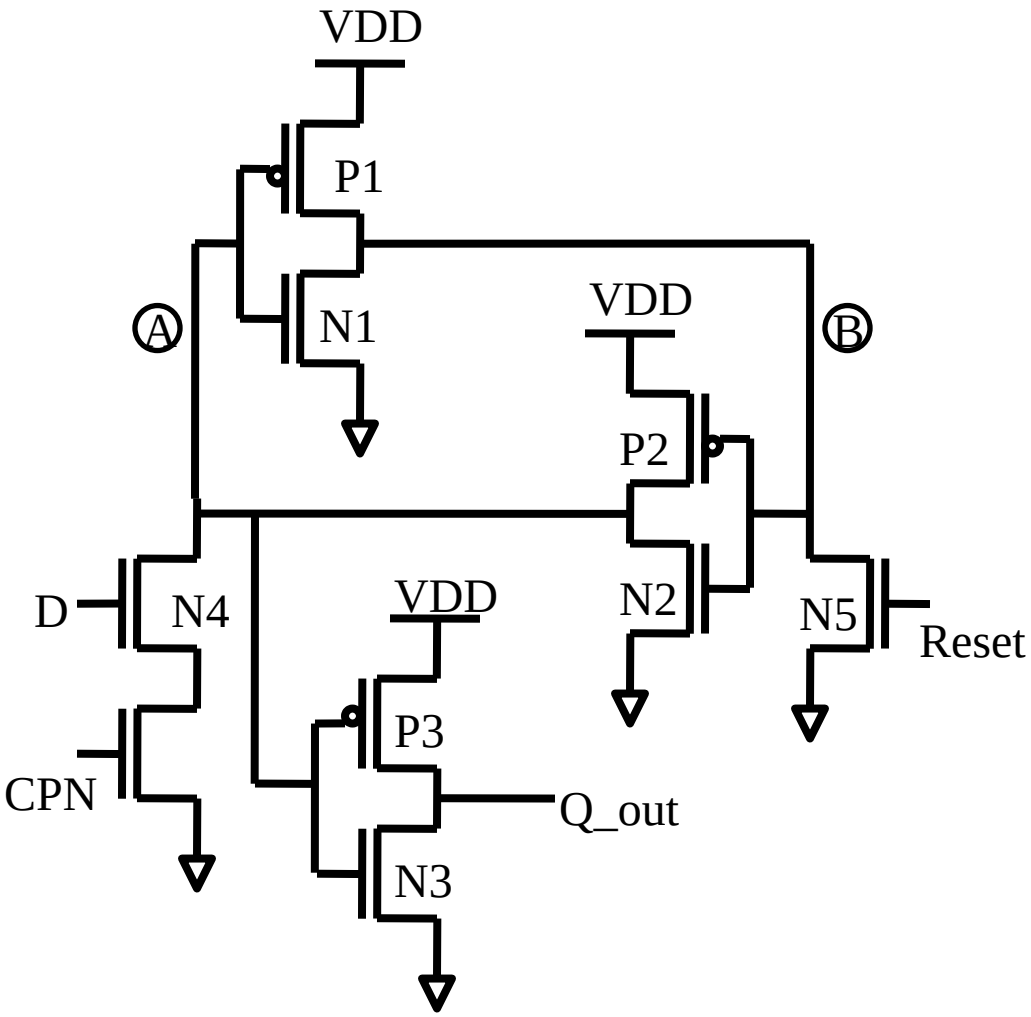
Standard cell library component

Synchronizer Circuits: Pseudo-NMOS Latch



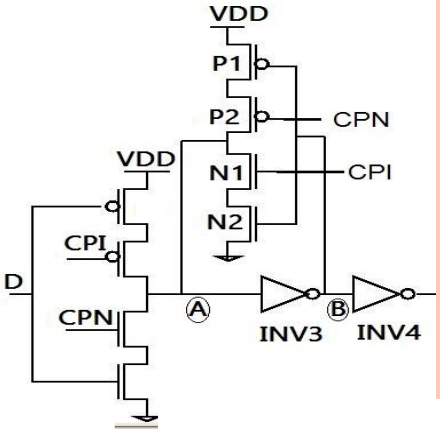
S. Yang, I.W. Jones and M. Greenstreet, "Synchronizer performance in deep sub-micron technology," *ASYNC 2011*

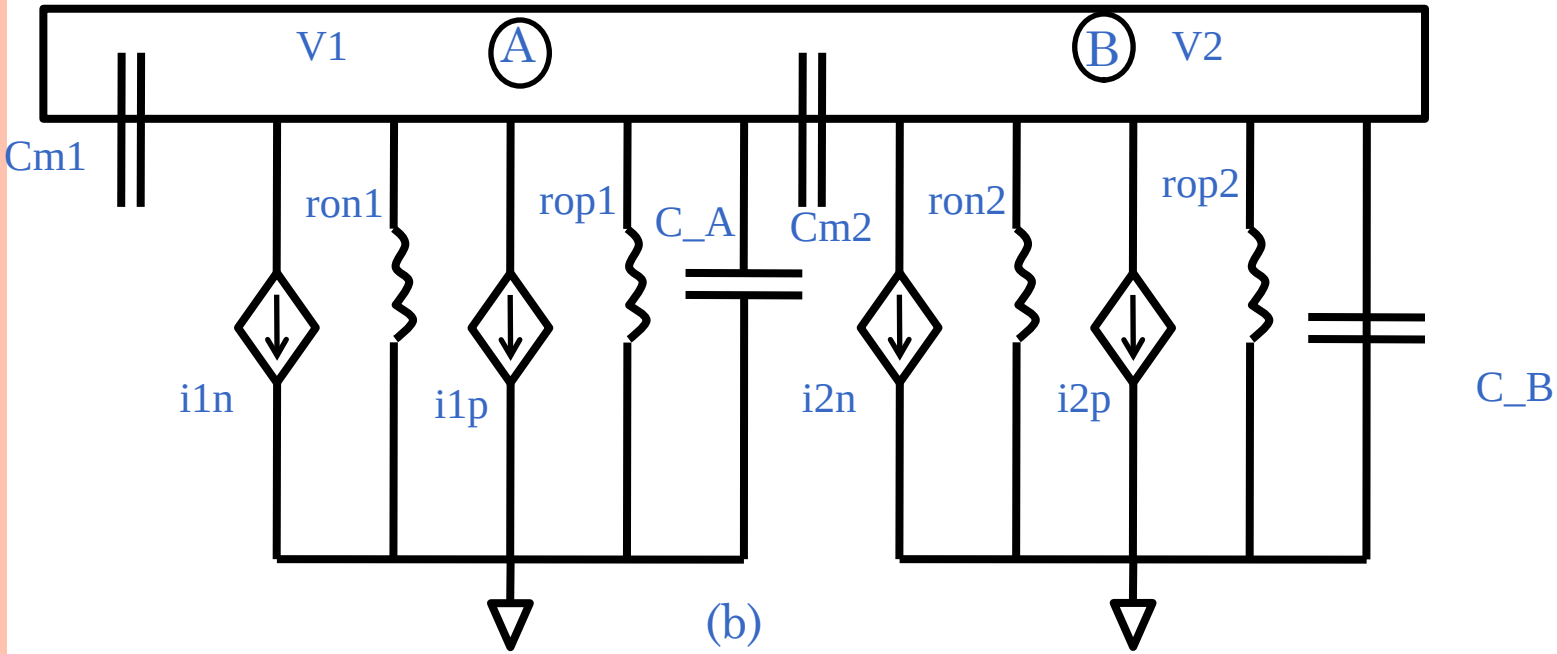
SYNCHRONIZER CIRCUITS: JAMB LATCH



J.Zhou, D.J.Kinniment, G. Russell, and A. Yakovlev, “”A Robust Synchronizer Circuit”, Proceedings of the ISVLSI’06, 2006

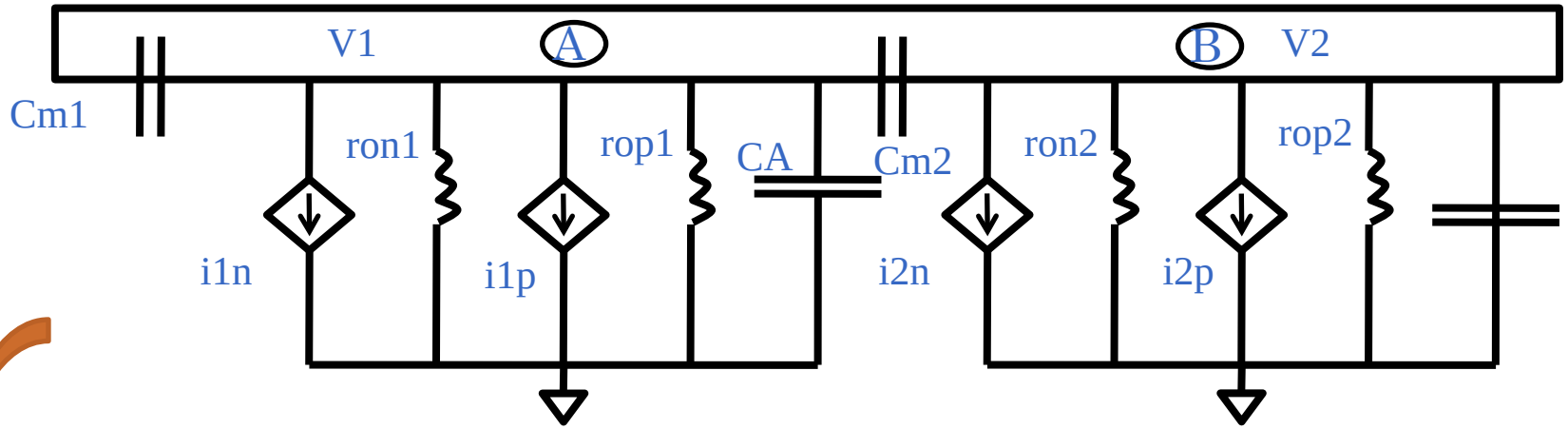
Analytical Models: Standard FF

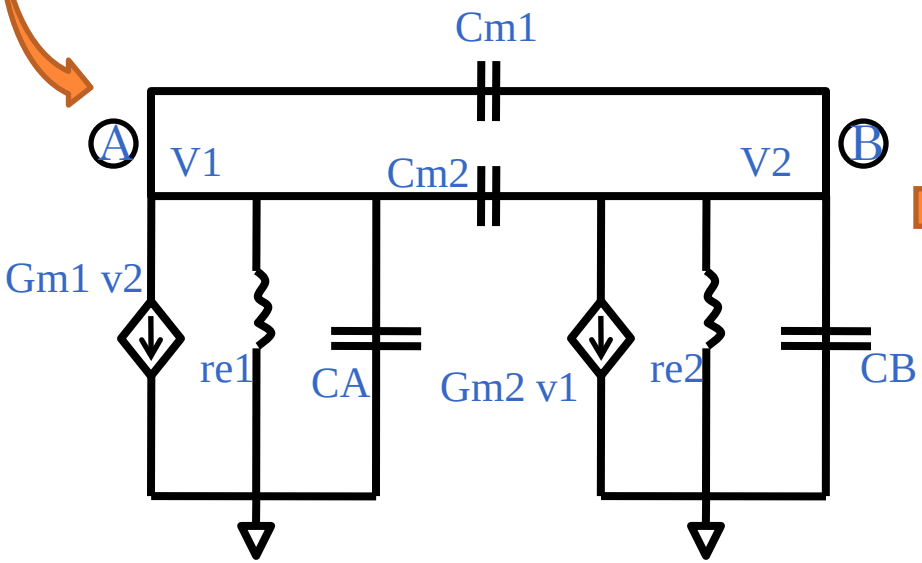


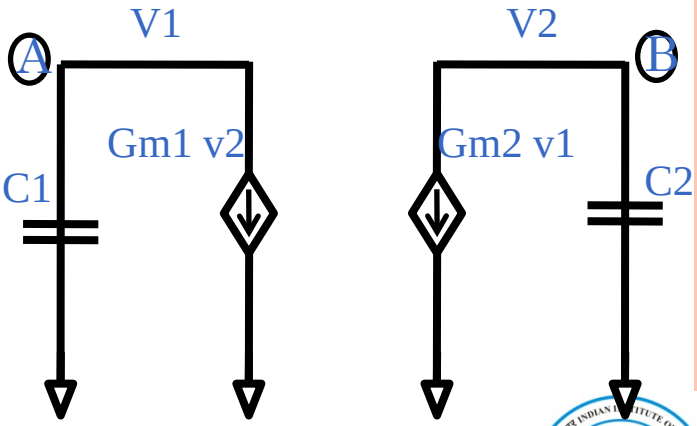


ron1, rop1, i1n, i1p : Correspond to path 1
ron2, rop2, i2n, i2p : Correspond to path 2

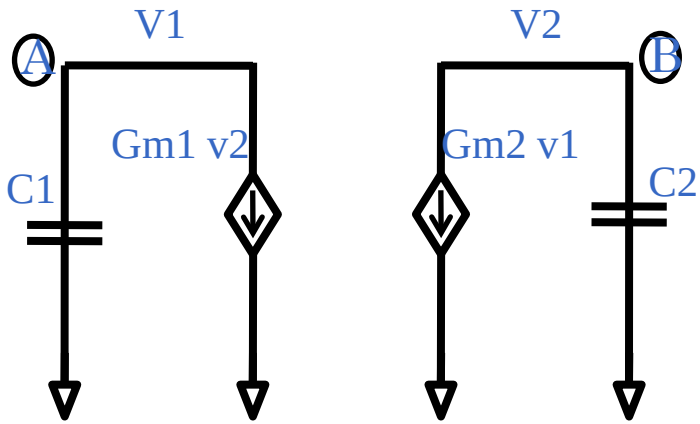
Approximation and Simplification







Small-Signal Analysis



$$G_{m1}v_2 + C_1\frac{dv_1}{dt} = 0$$

$$G_{m2}v_1 + C_2\frac{dv_2}{dt} = 0$$

$$v_1(t) = v_m\, exp\,(\frac{t}{\tau}) \qquad \tau = \frac{\sqrt{C_1C_2}}{\sqrt{G_{m1}G_{m2}}}$$

$$G_{m_1} = g_{mn} + g_{mp}$$

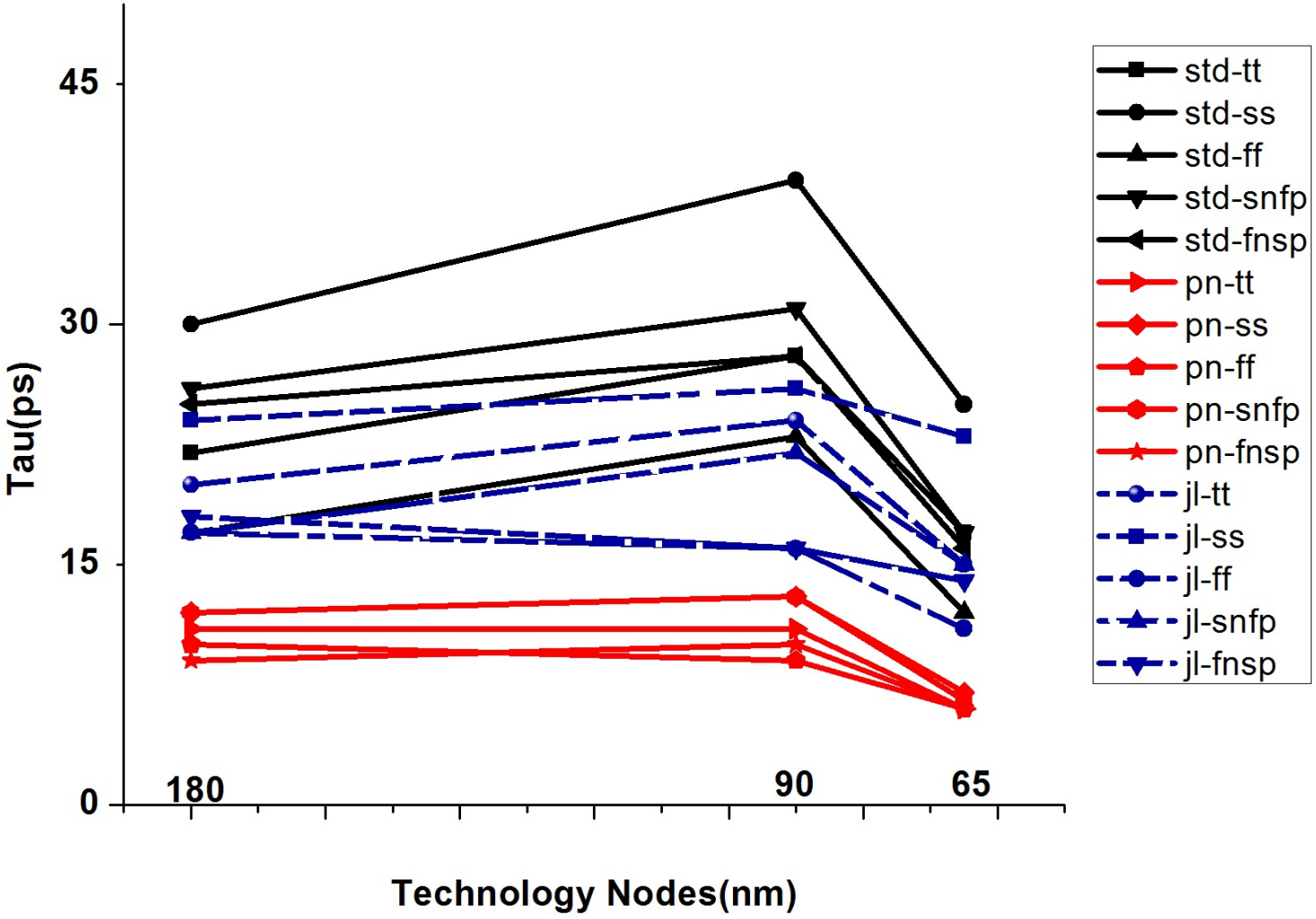
$$G_{m_1} = \left(\mu_n c_{oxn}\frac{\mathrm{N5}}{L}\cdot\frac{1}{1+\sqrt{a}} + \mu_p c_{oxp}\frac{\mathrm{P5}}{L}\cdot\frac{a}{1+\sqrt{a}}\right)\left(V_m - |v_{tp}| - \mathrm{v_{tn}}\right)$$

$$a = \frac{\mu_n c_{oxn}\frac{\mathrm{N5}}{L}}{\mu_p c_{oxp}\frac{\mathrm{P5}}{L}}$$

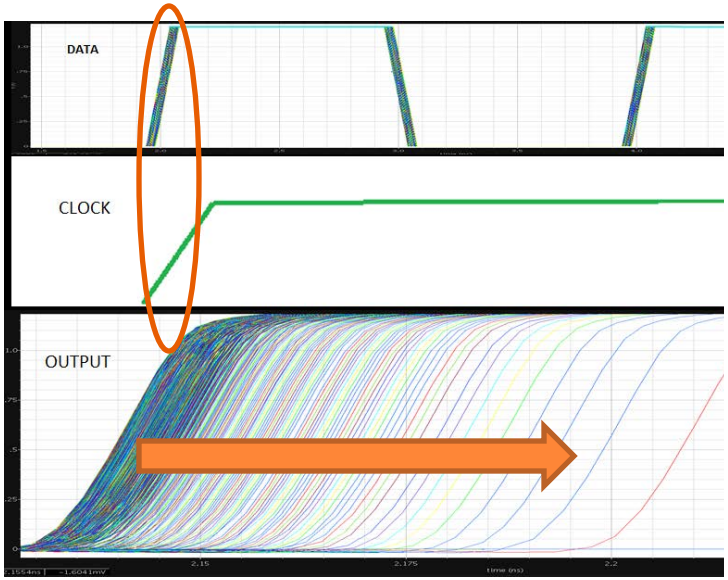
Analytical Plots

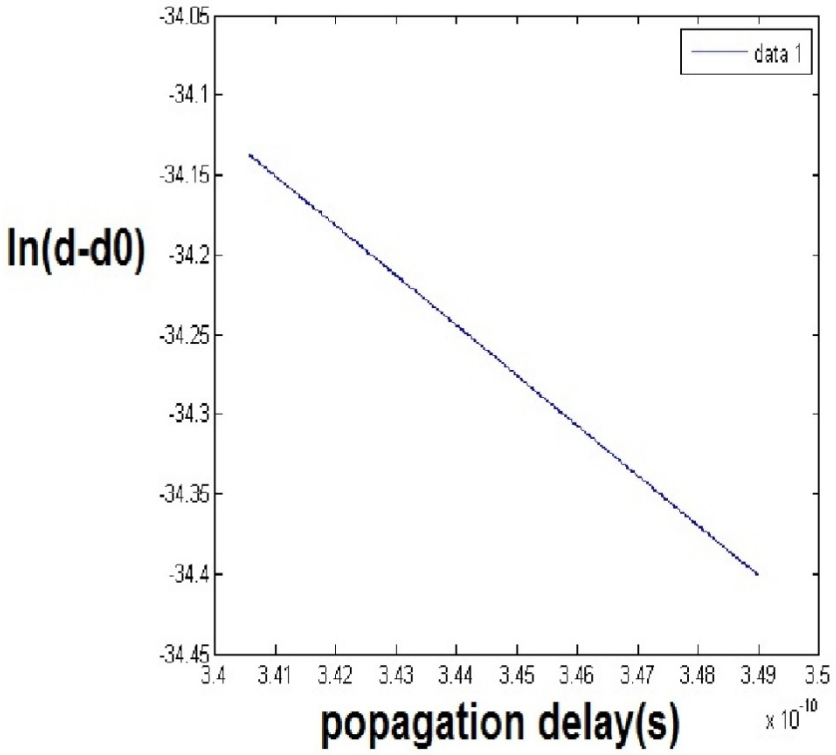
- Across different technology nodes: 180nm, 130nm, 90nm, 65nm
- Across multiple process corners: FF, SS, TT, SNFP, FNSP
- For 3 different synchronizer circuits

Analytical Plots

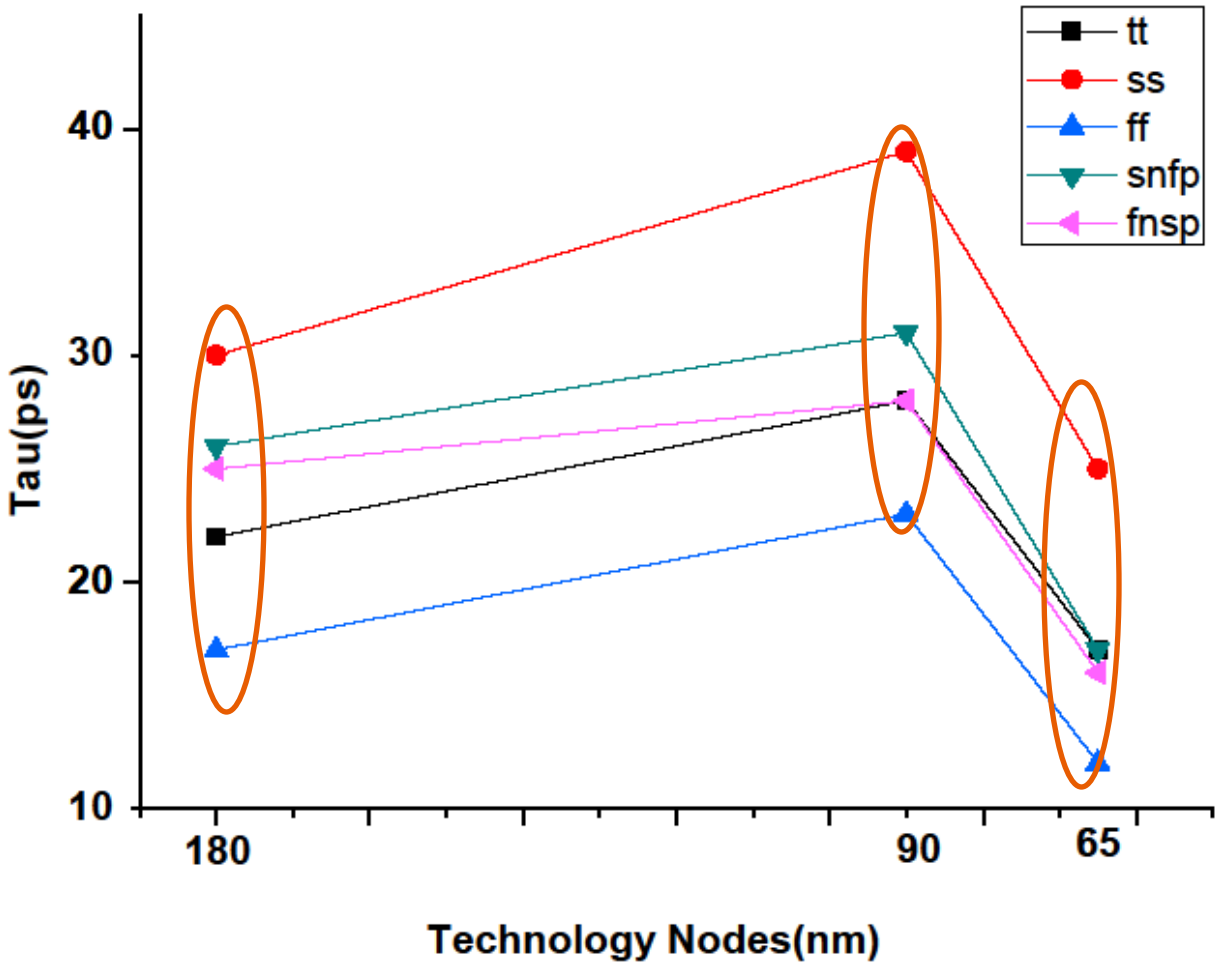


Simulation Study





Simulation Plots: Standard FF

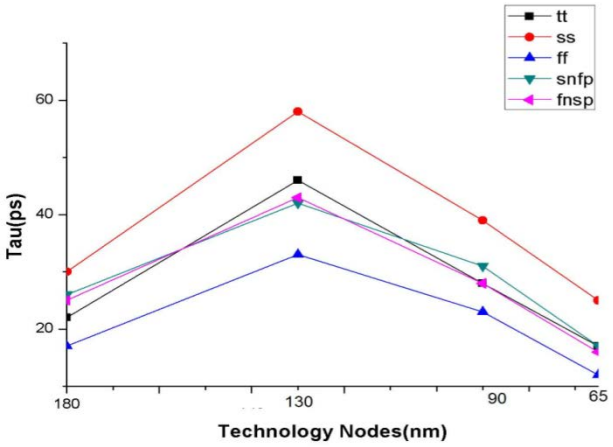


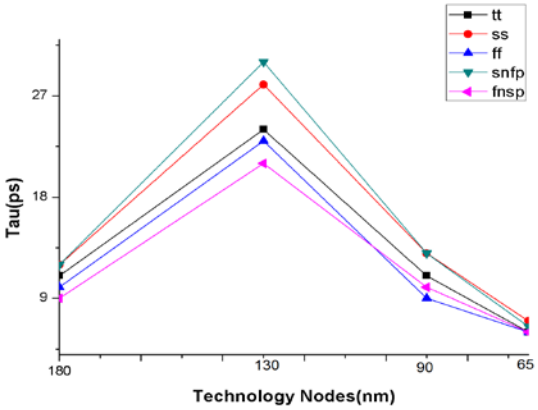
Standard design

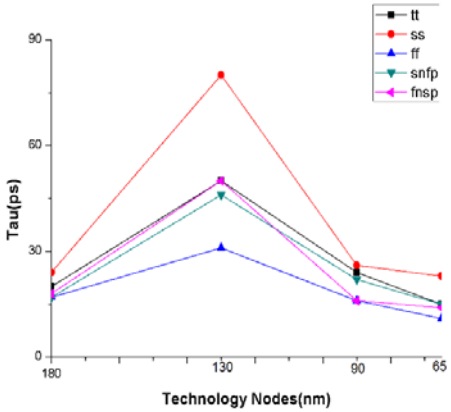
Pseudo-NMOS design

Jamb latch design

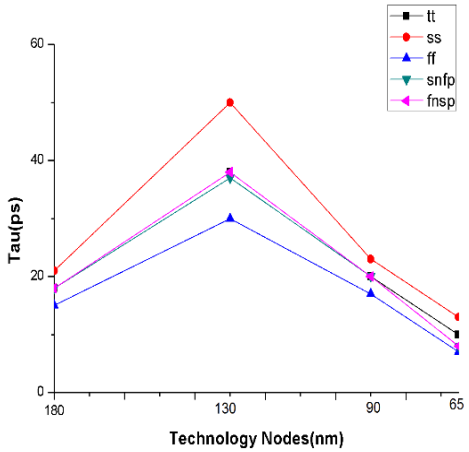
Simulated values

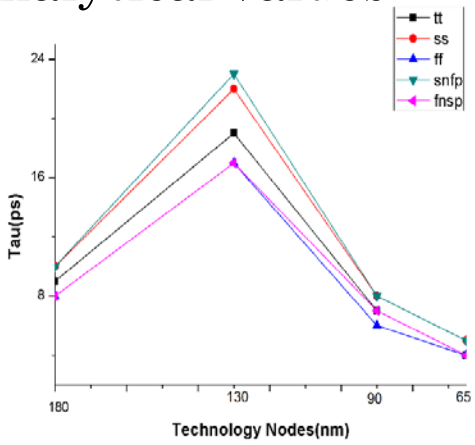


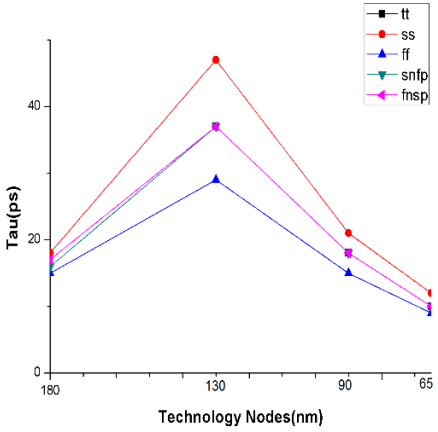




Analytical values







Summary and Observations

- Comparison of 3 different synchronizer circuits
  - At 4 technology nodes (180nm, 130nm, 90nm, 65nm)
  - Over all the 5 process corners
  - Using both analytical models and simulations
- Observations
  - Analytical models follows the simulation trends
  - Technology scaling observed in Simulations/Analysis different in Experiments (but more study required)
  - Pseudo-NMOS is more resilient to process variations (and scales better with technology!)

Thank You