GALS Methodology for Substrate Noise Reduction in Mixed-Signal Integrated Circuits

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Brandenburgische
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innovations
for high
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microelectronics

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Agenda

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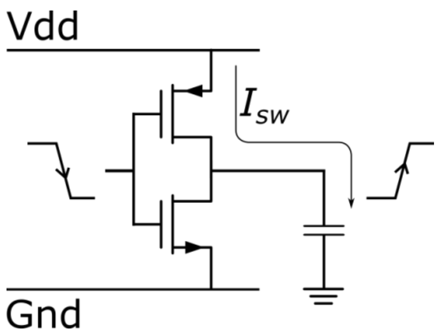
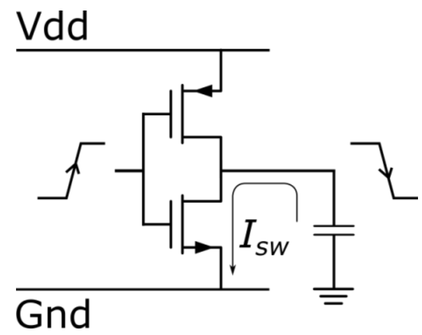
1	Introduction
2	Switching current spectrum optimization requirements for substrate noise reduction
3	Harmonic balanced partitioning
4	GALS partitioning algorithm for substrate noise reduction
5	Methodology for GALS partitioning
6	Conclusions and future work

Introduction – Substrate noise

- Gate switching:



output transition: 0 → 1



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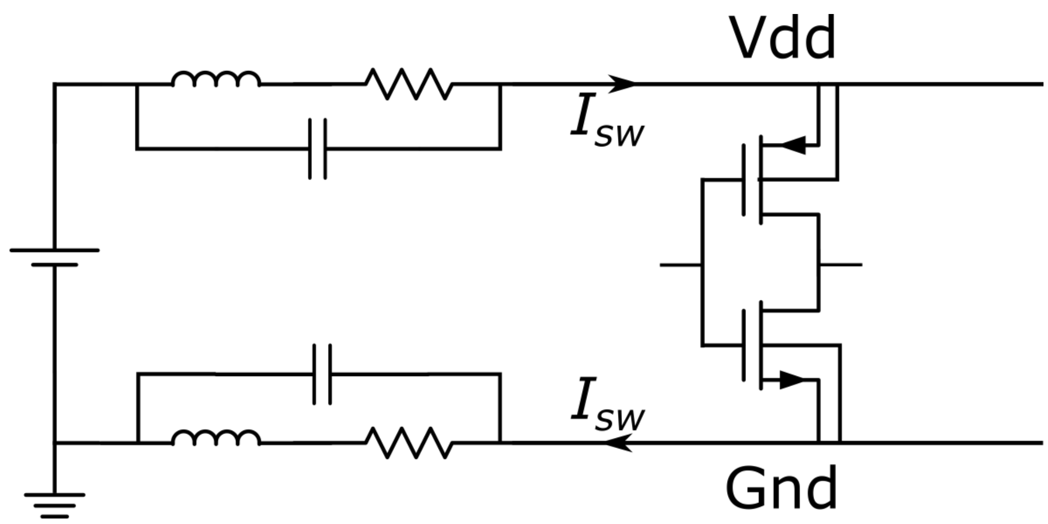

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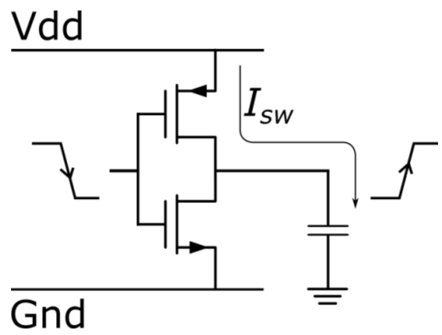

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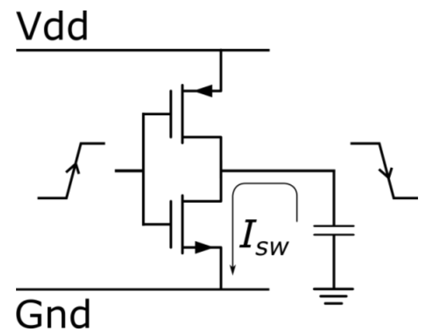

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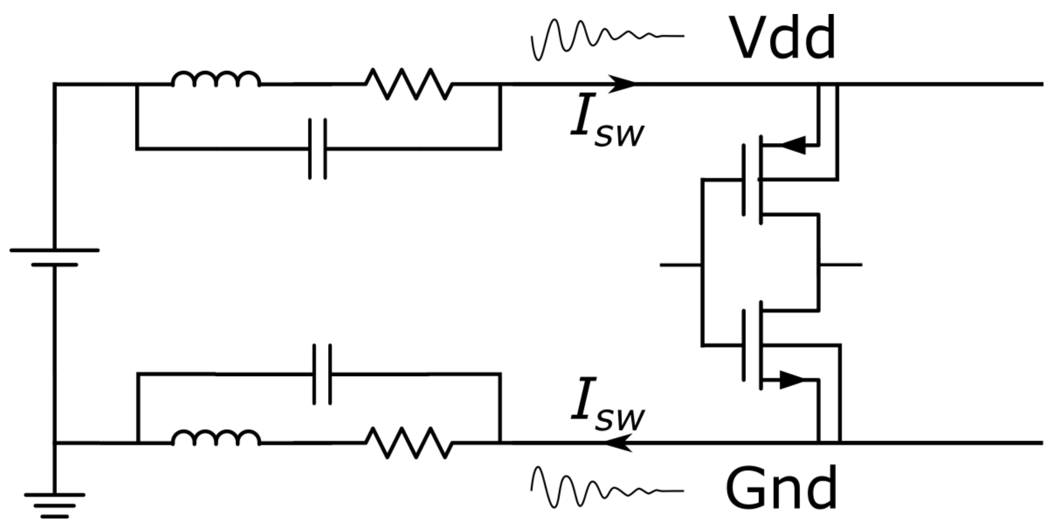
- Gate switching → Current surges in the supply and ground lines (switching current)
- Switching current → Voltage oscillations on supply and ground lines (supply and ground bounce)



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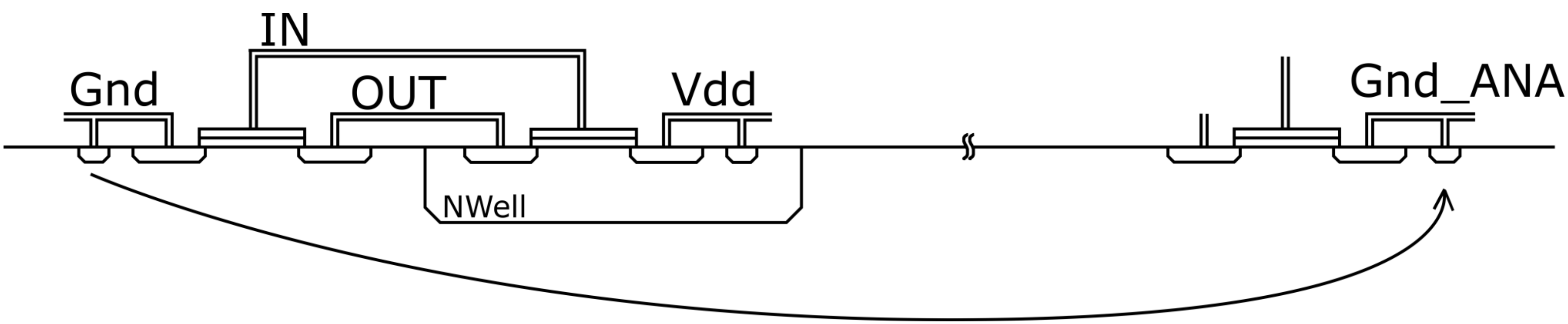
Introduction – Substrate noise

- Ground bounce → Voltage fluctuations in the substrate (substrate noise)



- **Direct coupling through substrate contacts → dominant coupling mechanism**
- This noise further propagates to the outputs of analog circuits, impacting the performance

Introduction – Substrate noise

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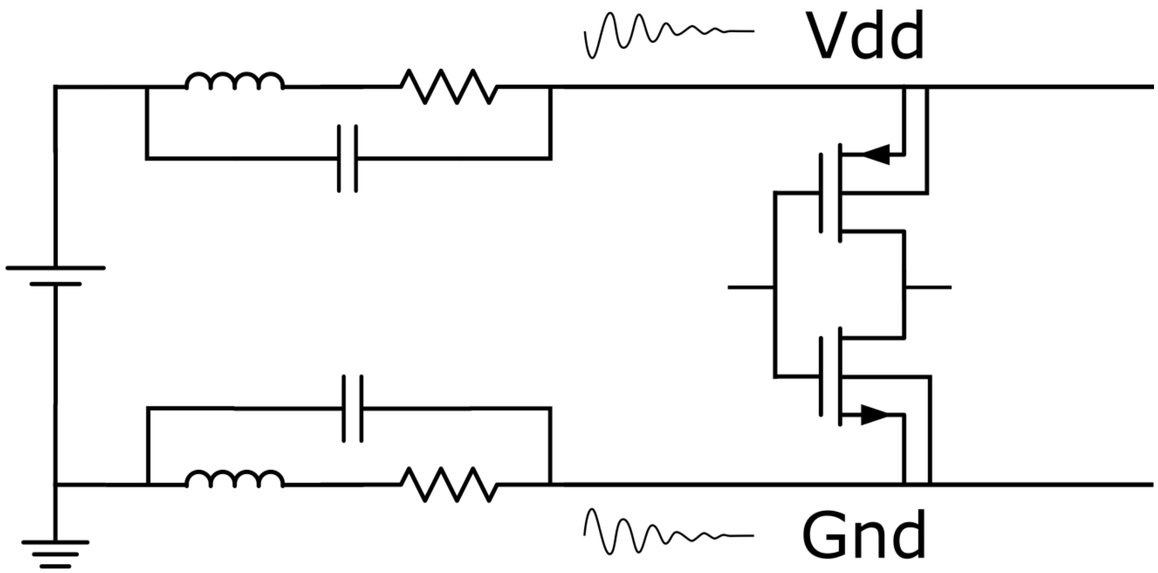

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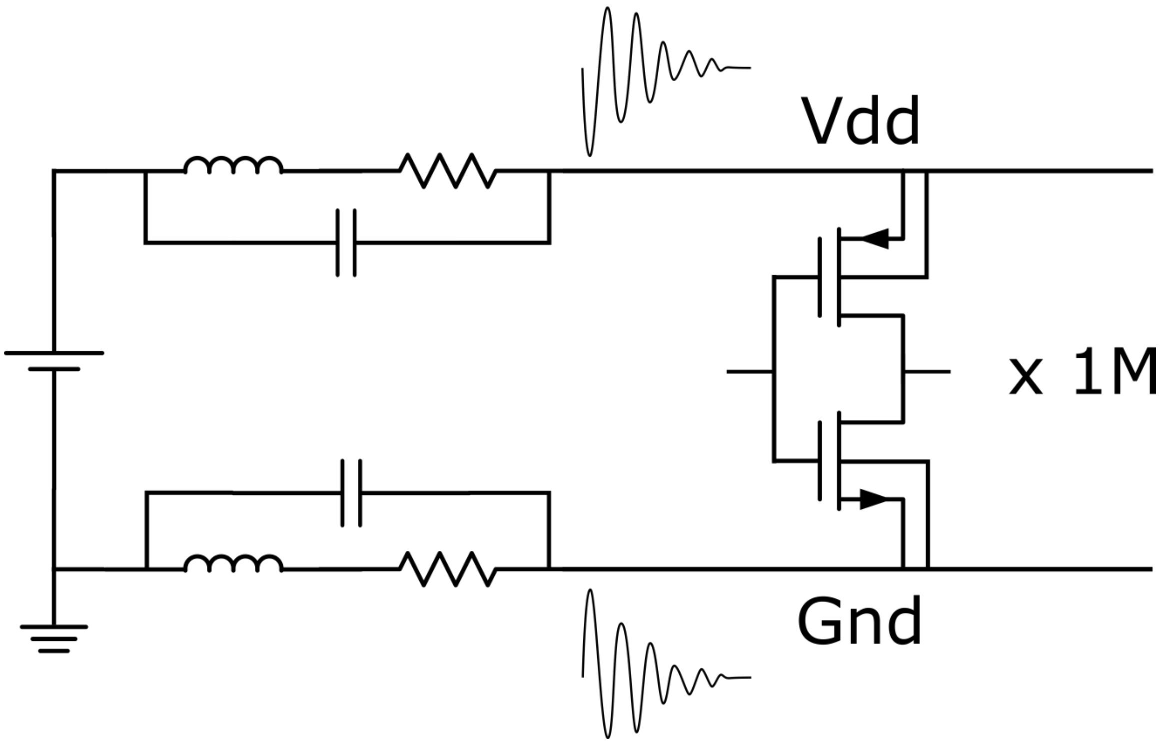

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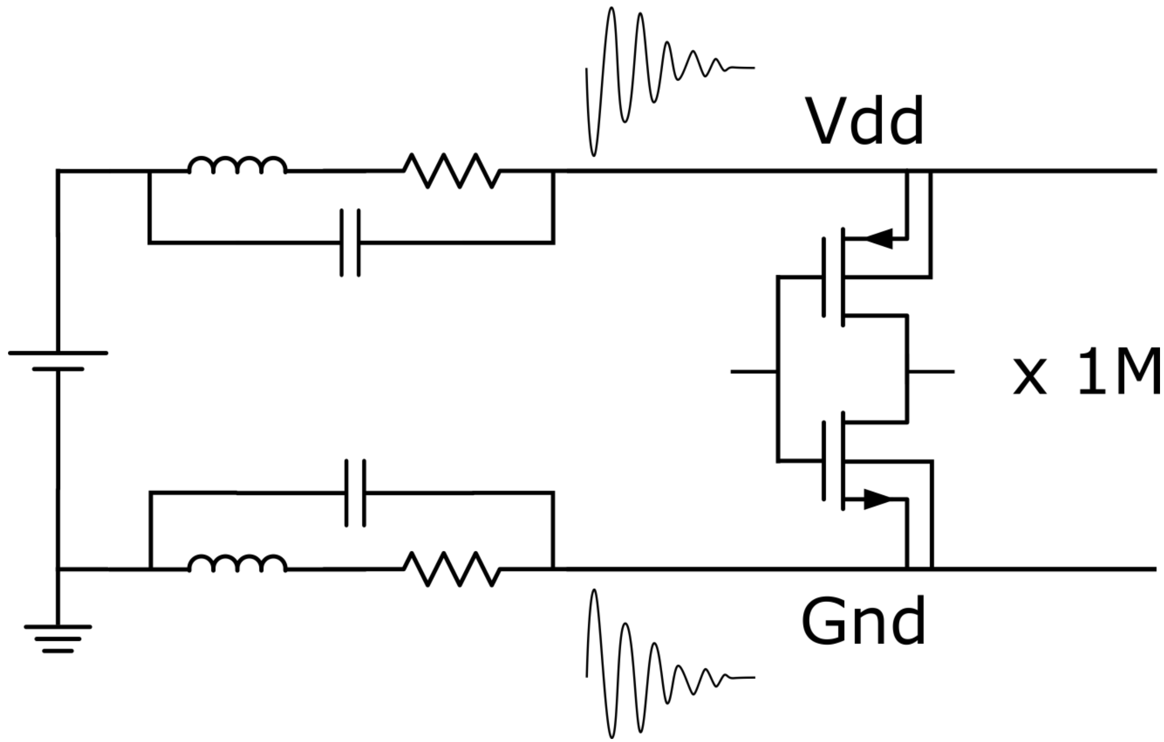

- Noise generation is, to a large extent, a system level effect, and thus can be addressed at system level

Introduction – Existing system level approaches for substrate noise reduction

- Spreading the switching activity in synchronous circuits
  - Introducing the intentional clock skew
  - Phase modulation of the clock
  - Pseudo-random clocking

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  - Plesiochronous clocking scheme with power-balanced partitioning
  - Spectral peak attenuation at the fundamental:

$$SPA_{dB} = 20\log \frac{A_{1,sync}}{\max\{A_{1m,GALS}\}} = 20\log M$$

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- The goal of this work:
  - Provide a corresponding methodology for **substrate noise** suppression

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- Substrate noise spectrum ($\boldsymbol{F}\{\boldsymbol{v}_{sub}\}$):

$$F\{v_{sub}\} = H_{sub}\, F\{v_{gb}\} = H_{sub} H_p\, F\{i_{sw}\} = H\, F\{i_{sw}\}$$

$\boldsymbol{F}\{\boldsymbol{v}_{gb}\}$ – ground bounce spectrum

$\boldsymbol{H}_{sub}$ – substrate transfer function (from aggressor substrate contacts to the victim)

$\boldsymbol{F}\{\boldsymbol{i}_{sw}\}$ – switching current spectrum

$\boldsymbol{H}_{p}$ – package & PDN transfer function (from switching current to ground bounce)

$\boldsymbol{H}$ – total package & PDN and substrate transfer function
(from switching current to the victim)

  - $\boldsymbol{H}$ usually pass-band → dominant components at higher frequency

Spectrum optimization requirements for substrate noise reduction

- Spectrum optimization goal:
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  - LNA:
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- Requirements:
  - Noise suppression at higher frequencies
  - Possibility of frequency selective noise suppression covering multiple frequency bands

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$$F_n\{v_{subm}\} = H_{nm}\, F_n\{i_m\} \quad , \quad F_n\{v_{sub}\} = H_n\, F_n\{i\}$$

same power domain for all the partitions + plesiochronous desing →
→ $H_{n1} \approx H_{n2} \approx \cdots \approx H_{nm} \approx H_n$

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    - **switching current peak attenuation = substrate noise peak attenuation**

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$$\rightarrow H_{n1} \approx H_{n2} \approx \cdots \approx H_{nm} \approx H_n$$

$$SPA_{dB} = 20\log\frac{|F_n\{v_{sub}\}|}{\max\{|F_n\{v_{subm}\}|\}} \approx 20\, log\frac{|F_n\{i\}|}{\max\{|F_n\{i_m\}|\}}$$

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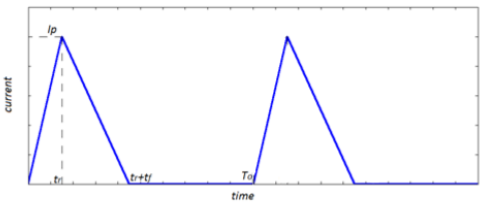
- Analysis of the impact of that approximation:
  - Switching current modeled as a periodic triangular pulse
  - Spectrum calculated by applying a nominal frequency, and a frequency with a small offset



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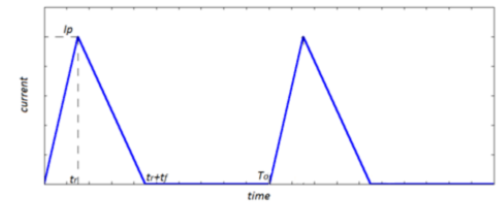

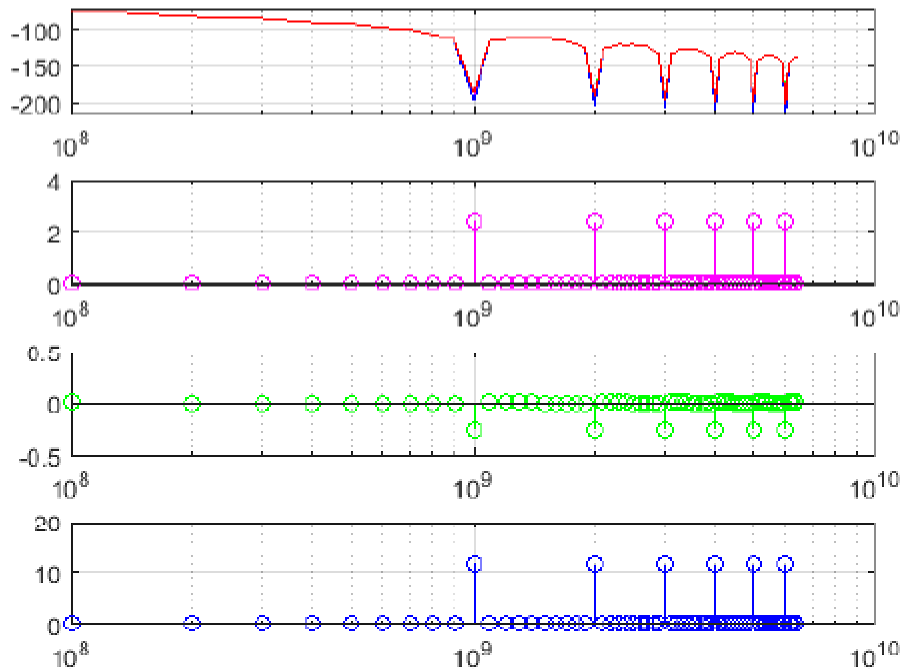

switching current spectrum envelope

error in dB, 1% frequency offset

error in dB, 3% frequency offset

error in dB, 5% frequency offset

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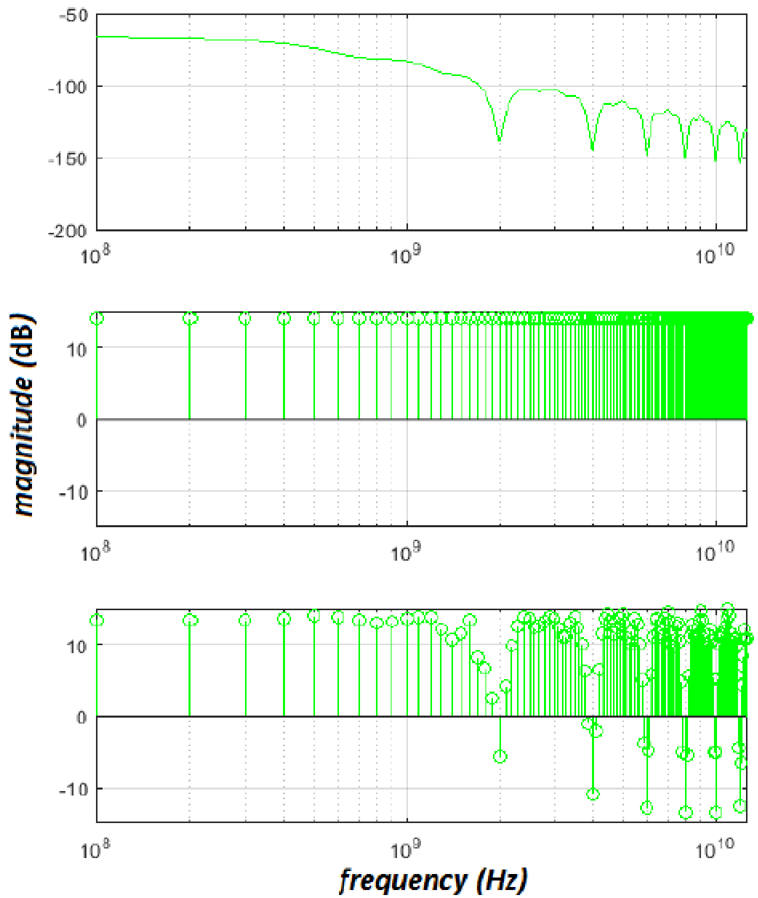
- Analysis of the impact of plesiochronous approximation - continuation:
  - Harmonic balancing applied at all frequencies, attenuation calculated



synchronous system –
- spectrum envelope

attenuation calculated by applying the plesiochronous approximation

attenuation calculated without applying the plesiochronous approximation

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- Finite granularity of the initial synchronous design
  - Design consists of a finite number of blocks
  - Partitioning = Assigning the blocks to partitions
  - Even if suppression at only one harmonic is targeted,

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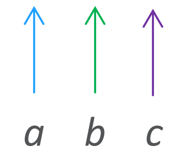
Example:
- three blocks
- two partitions
- one harmonic



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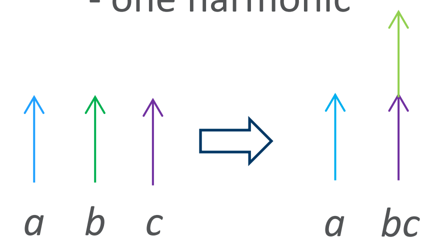

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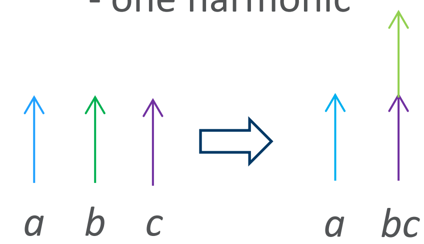

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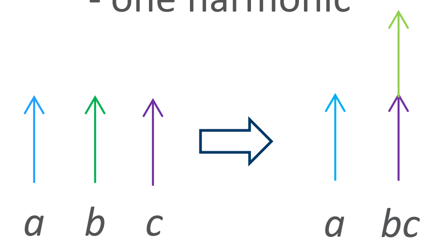

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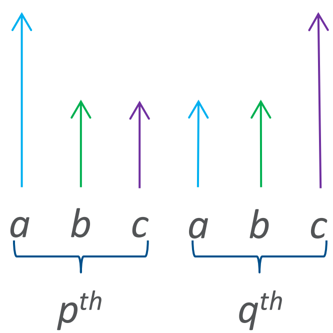

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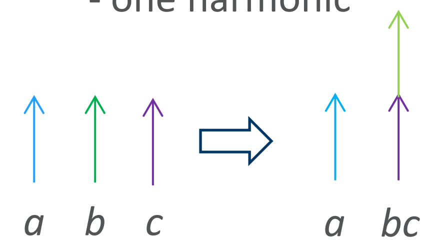

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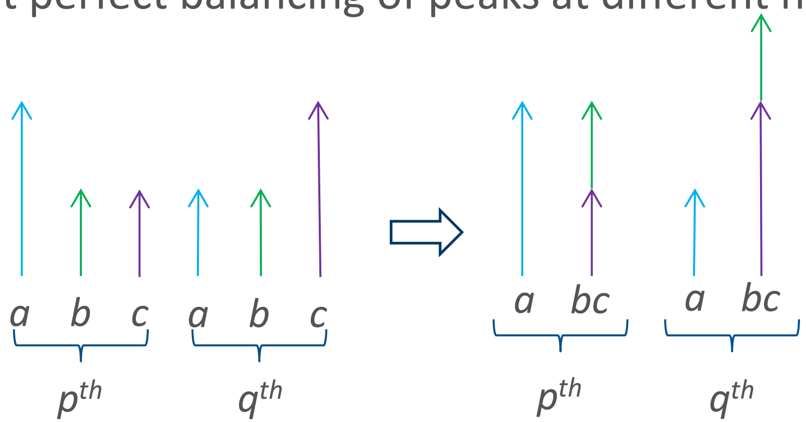

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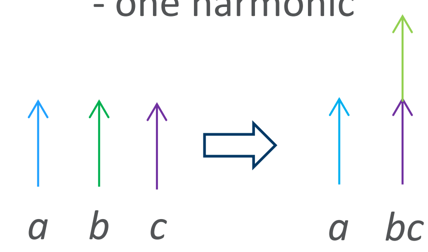

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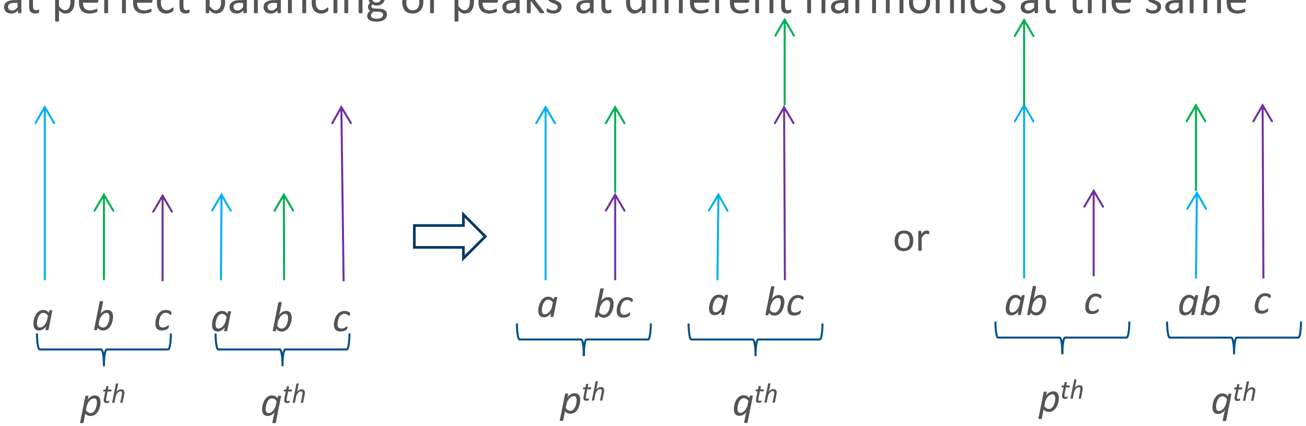

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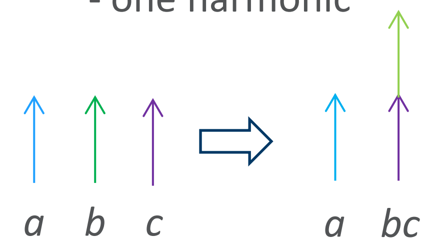

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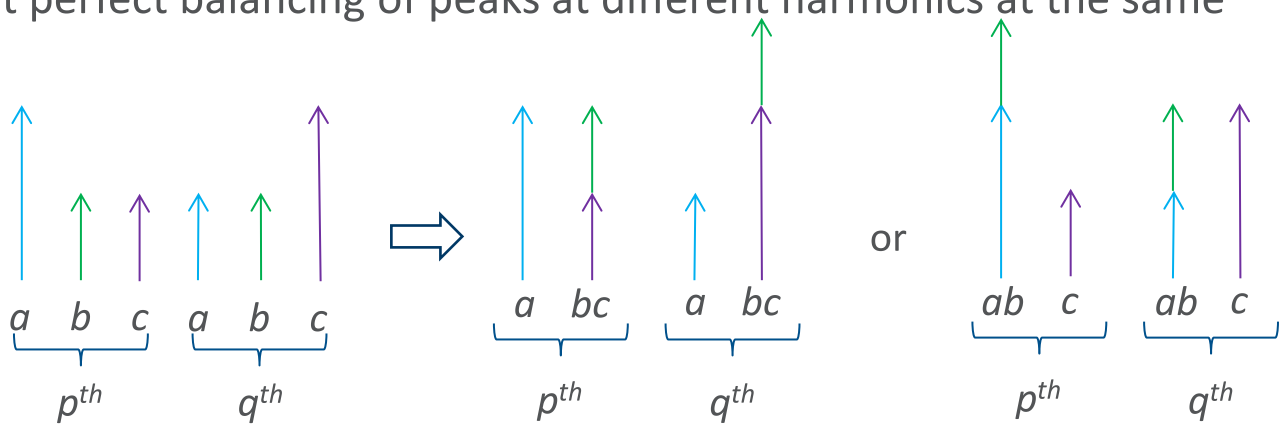
- three blocks
- two partitions
- two harmonics, p^{th} and q^{th}



- Find the partitioning which is the closest to the perfect harmonic balancing

Harmonic balanced plesiochronous design in practice

- For searching through combinations, the simulated annealing algorithm was used
  - Chose initial combination

Example: *blocks*: ***a b c d e f g h***

initial combination: {***a c f h***} {***b d e g***}

Harmonic balanced plesiochronous design in practice

- For searching through combinations, the simulated annealing algorithm was used
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  - Pick a random „neighboring combination“

Example: *blocks*: ***a b c d e f g h***

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neighboring combination: {***a c h***} {***b d e f g***}

Harmonic balanced plesiochronous design in practice

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  - Chose initial combination
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  - If the new combination is better – take it

Example: *blocks*: ***a b c d e f g h***

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  - If the new combination is worse – take it only with some probability, which gets smaller with the number of iterations

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initial combination: {*a c* ***f*** *h*} {*b d e g*}
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  - If the new combination is better – take it
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- Cost function to decide whether the combination is better or worse
  - Least total harmonics power
  - Least mean square difference to the theoretically „perfect partitioning“
  - Least power of the strongest harmonic

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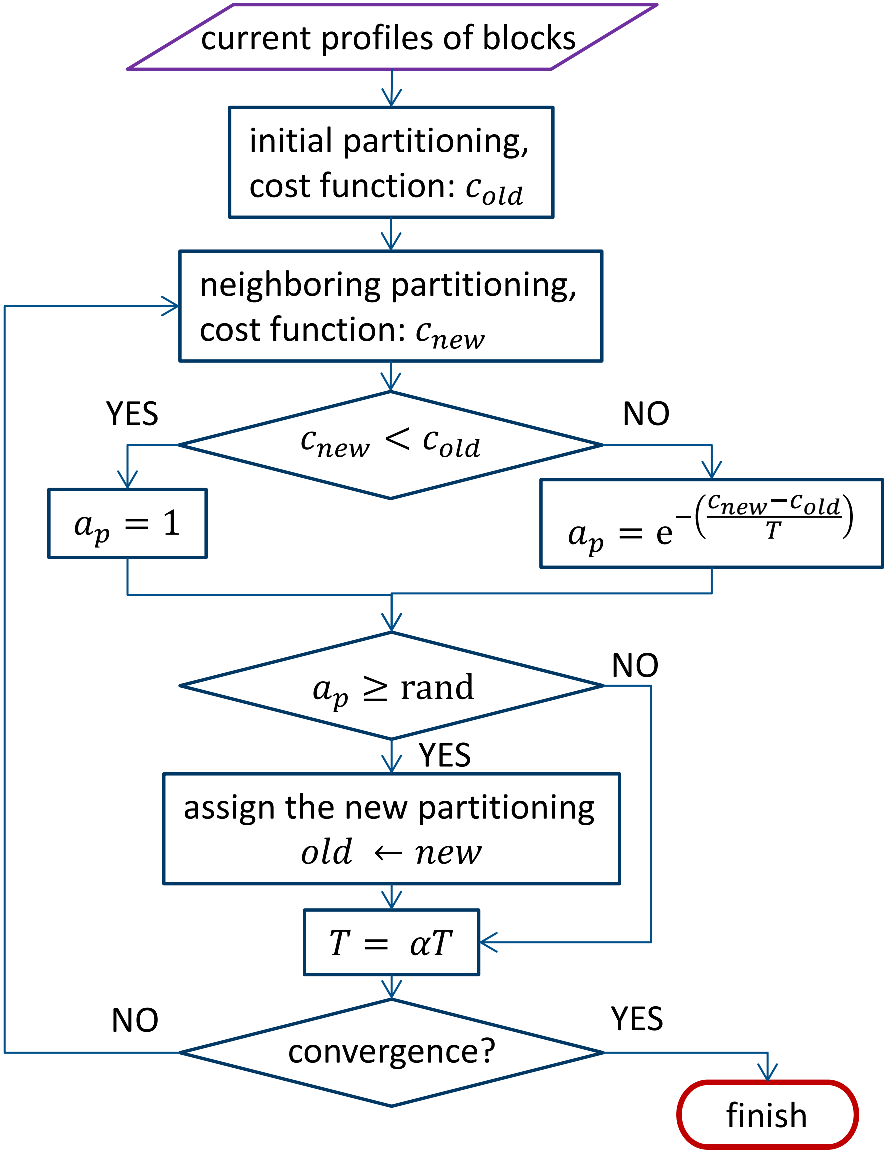
  - Least power of the strongest harmonic

- Calculate the cost function only for the frequency band(s) targeted for optimization

  → Frequency selective attenuation

Harmonic balanced plesiochronous design in practice



Notes:

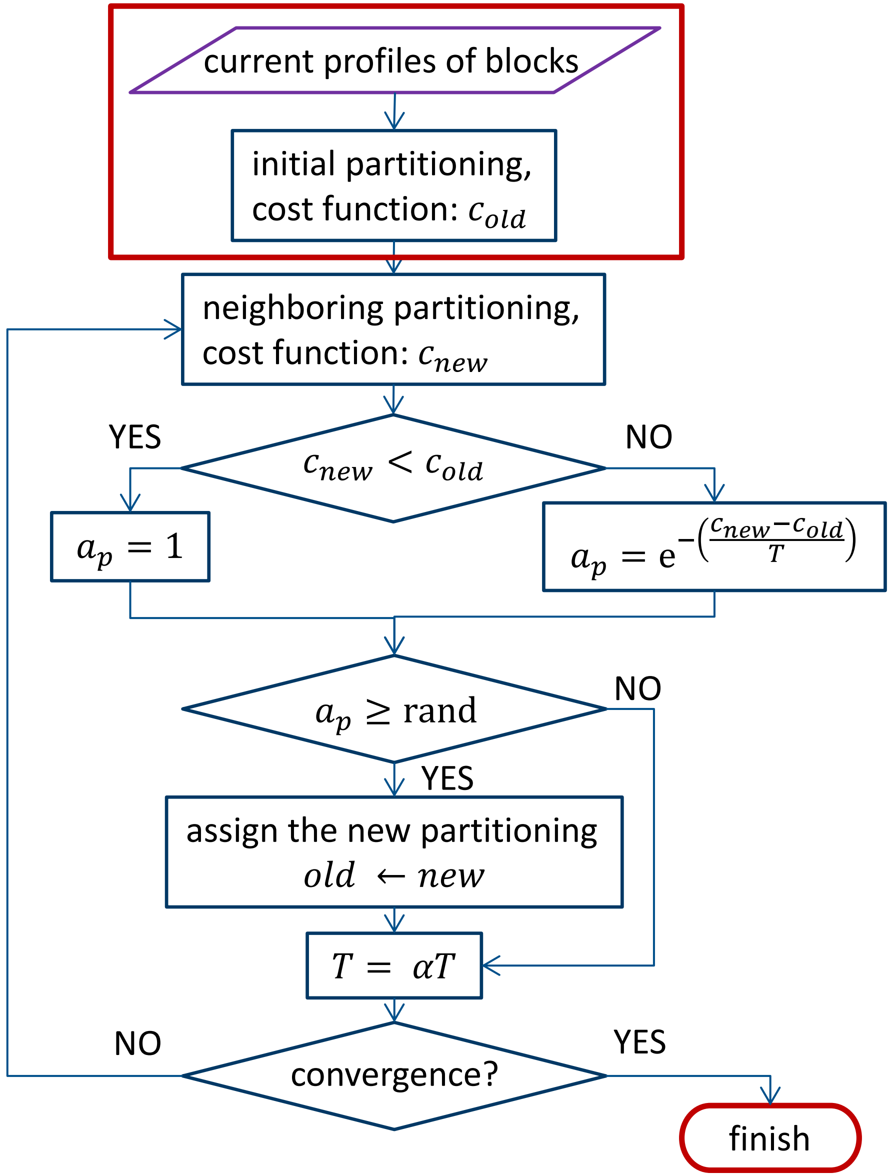
a_p – acceptance probability of the new partitioning

T – *"temperature", a parameter which gets reduced at each iteration*

$0 \leq \text{rand} \leq 1$

$\alpha < 1$

Harmonic balanced plesiochronous design in practice



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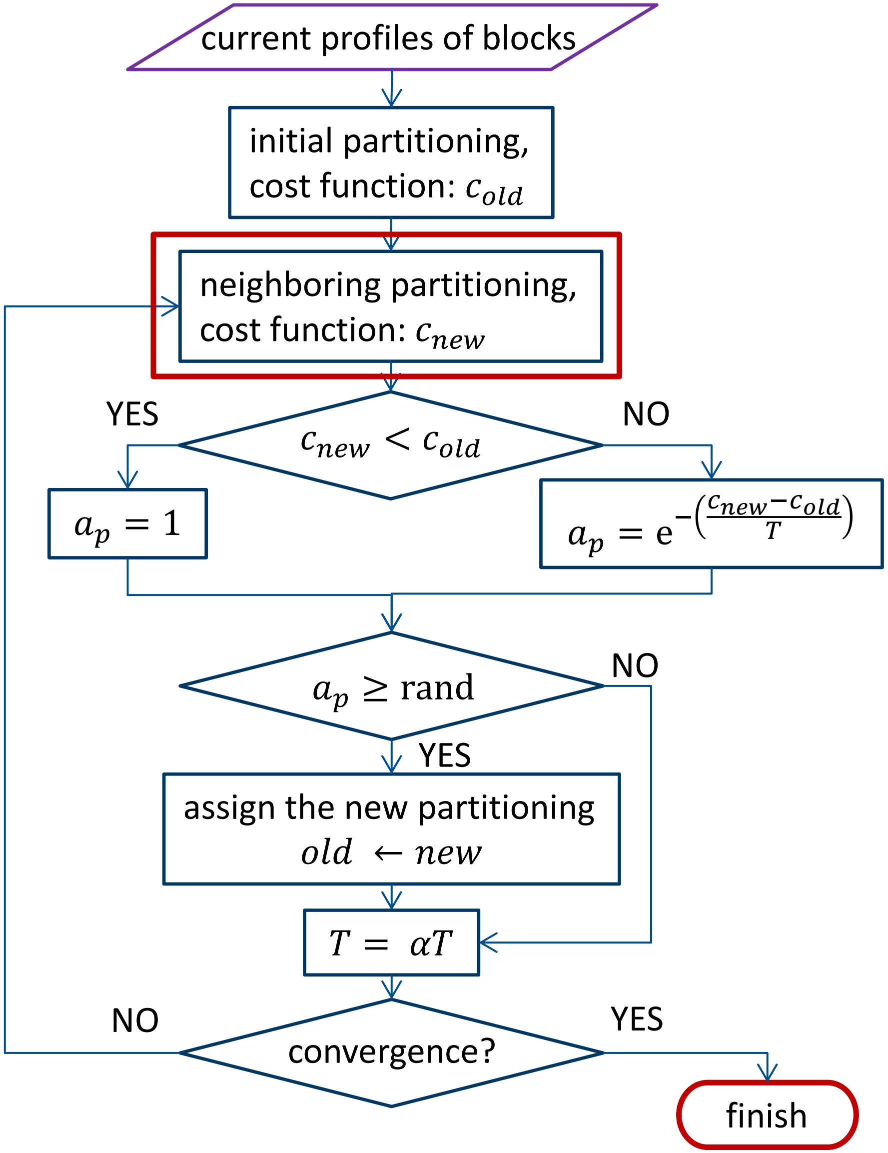

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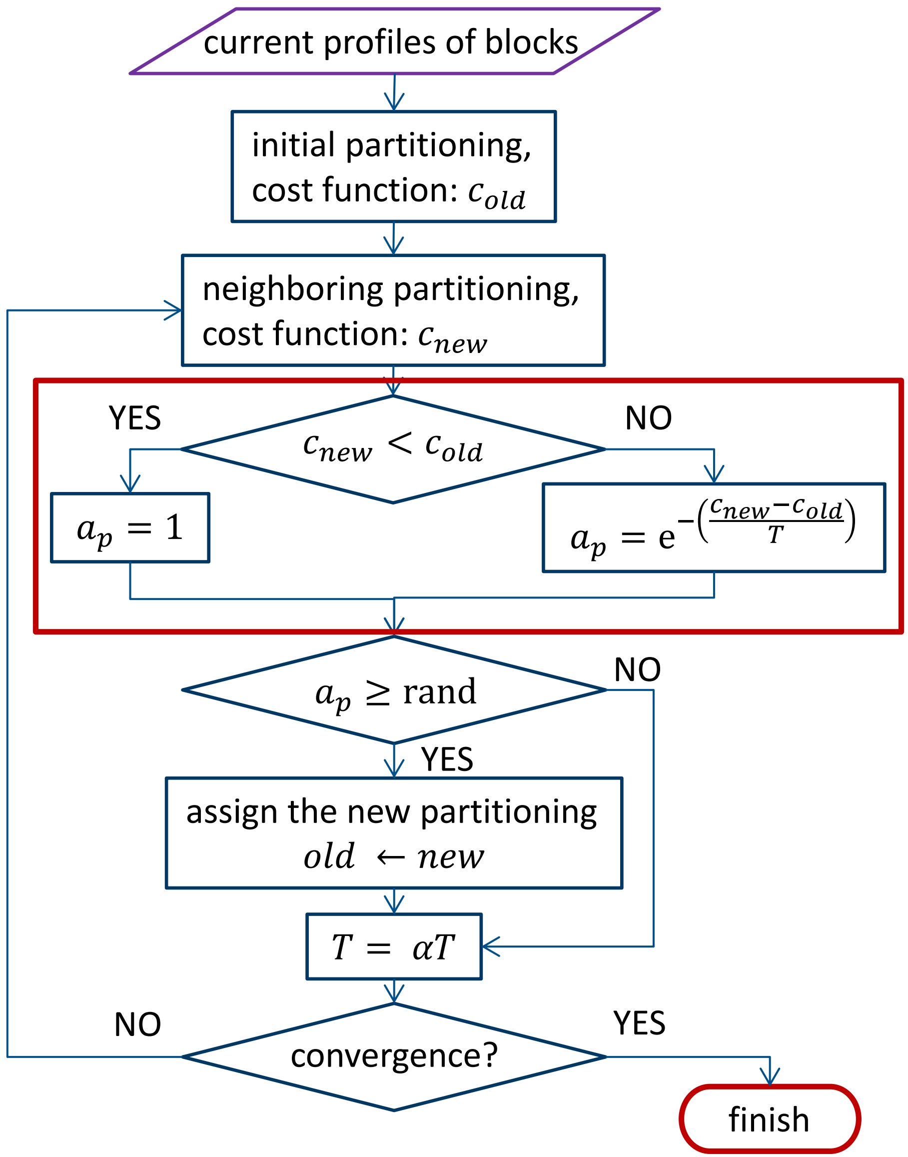

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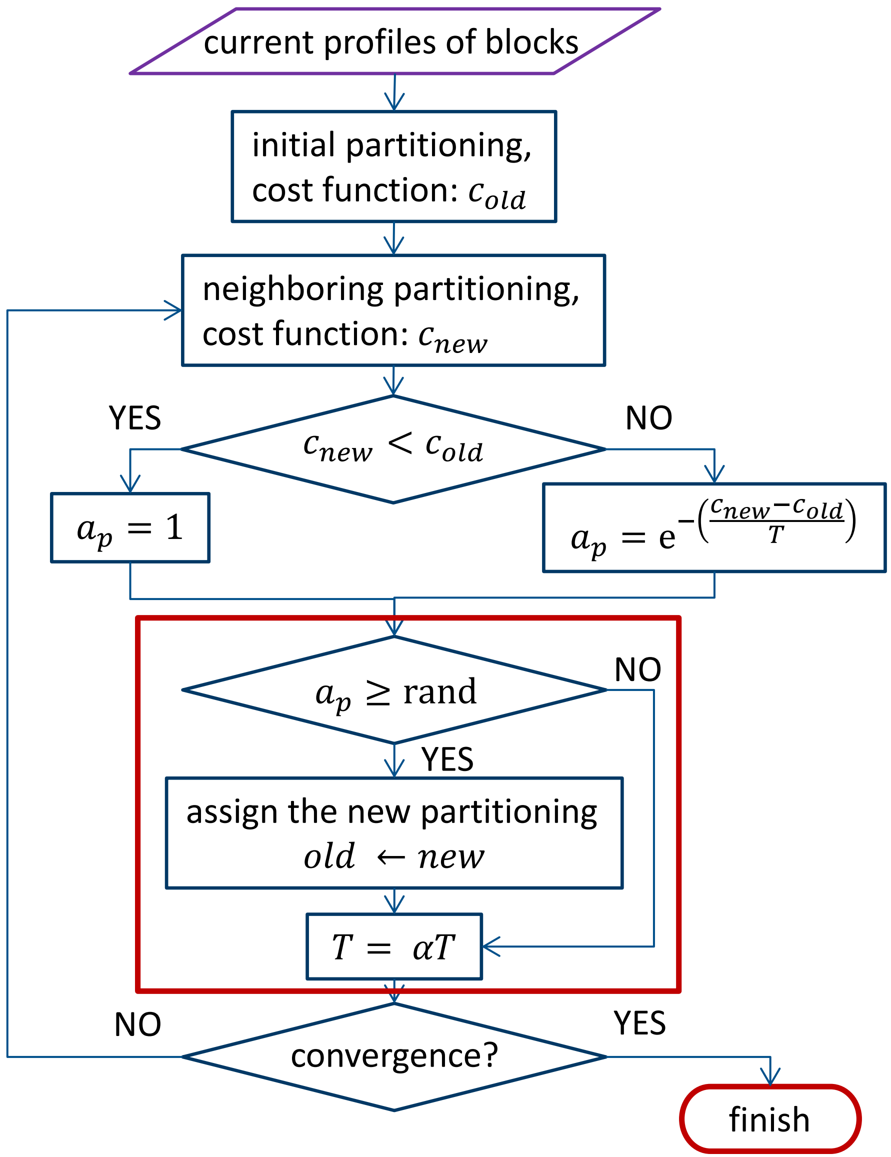

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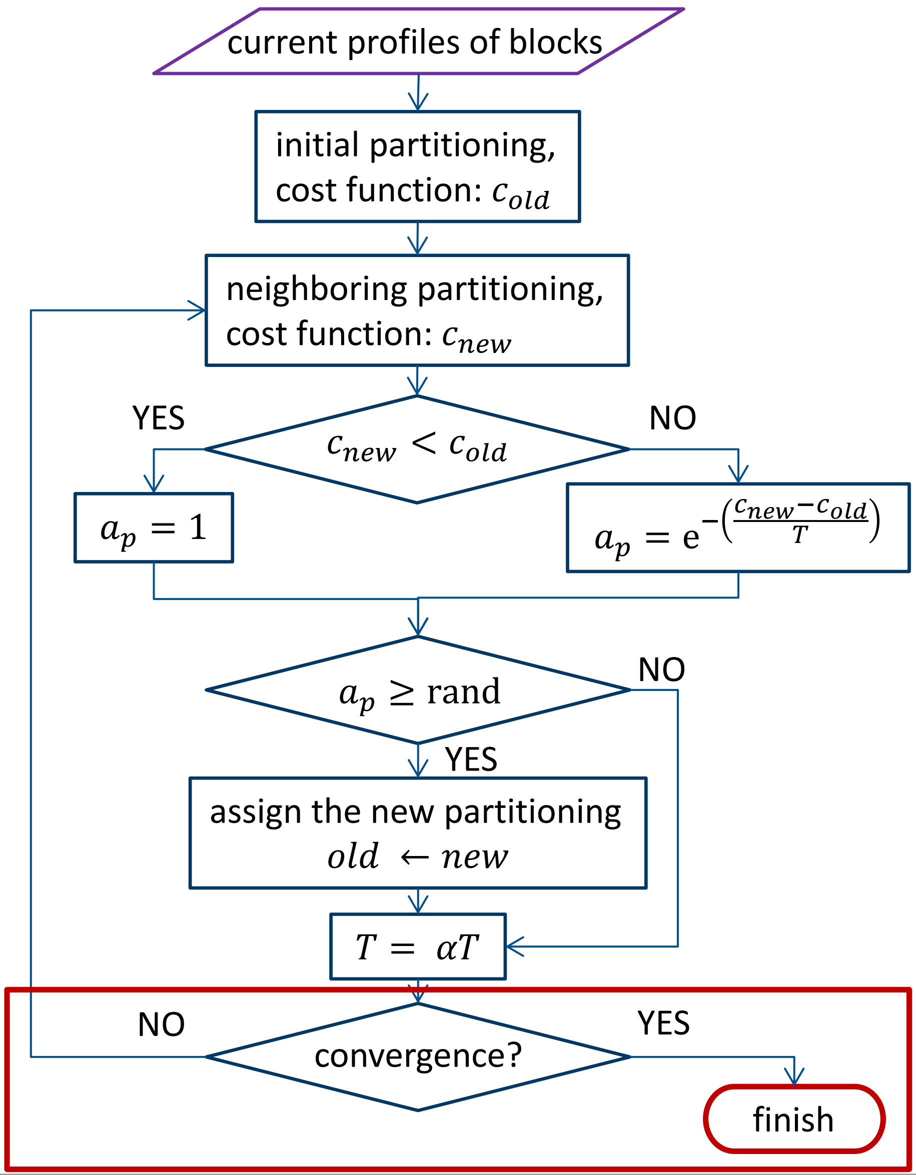

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Numerical evaluation of the methodology in MATLAB

- Block waveforms: periodic triangular pulses
- Random rise times (range: 0-20% T_{sclk}) and fall times (range: 0-80% T_{sclk})
- Random current peak (range: 0 - 1 mA)
- 40 blocks, 5 partitions (theoretically maximum attenuation: 13.98 dB)
- Frequency offsets for the partitions: -4%, -2%, 1%, 3%, 5%

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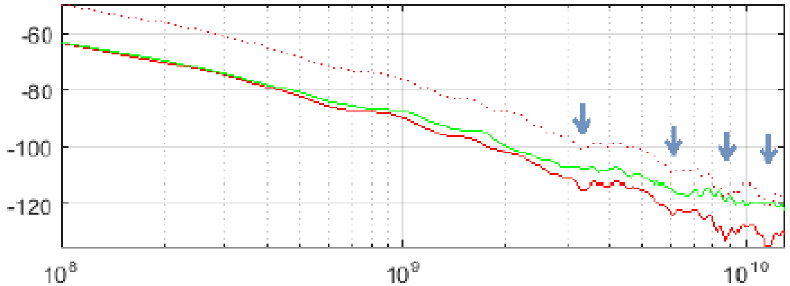
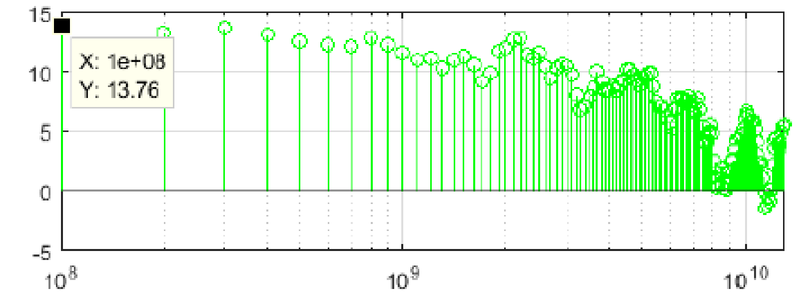
- Optimization on all the harmonics:



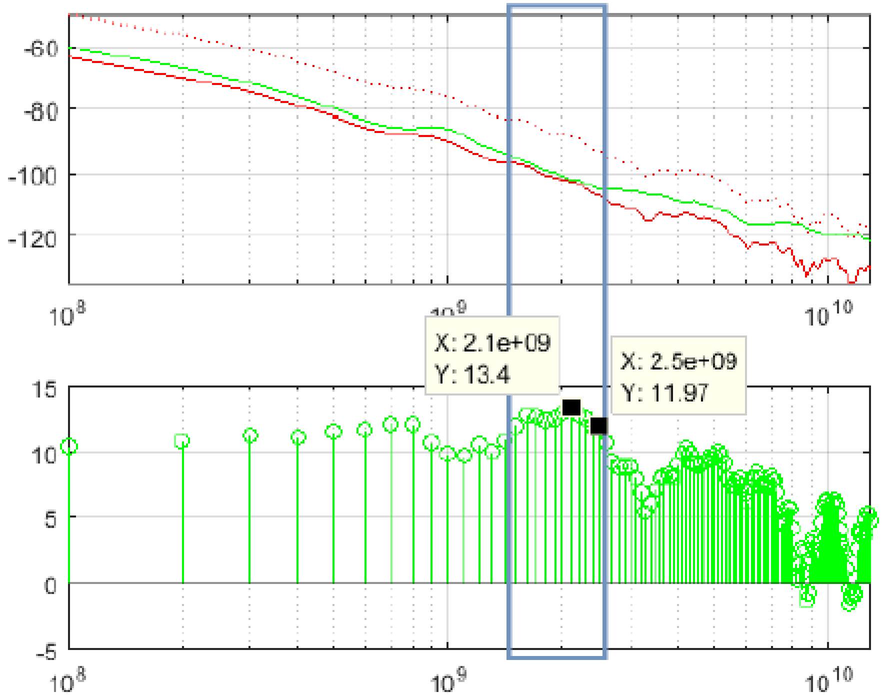
spectrum envelopes:
red dotted – synchronous
red – GALS, "perfect" partitioning
green – GALS



spectral peak attenuation

Numerical evaluation of the methodology in MATLAB

- Optimization in [1.5 GHz – 2.5 GHz] frequency band:



spectrum envelopes:

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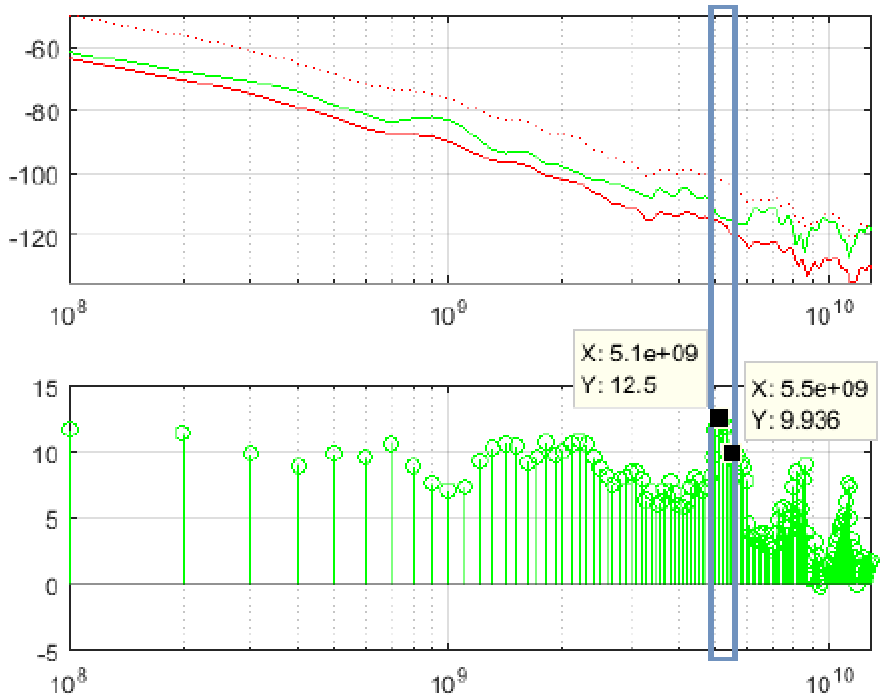
spectral peak attenuation

Numerical evaluation of the methodology in MATLAB

- Optimization in [5 GHz – 5.5 GHz] frequency band:



spectrum envelopes:
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red – GALS, "perfect" partitioning
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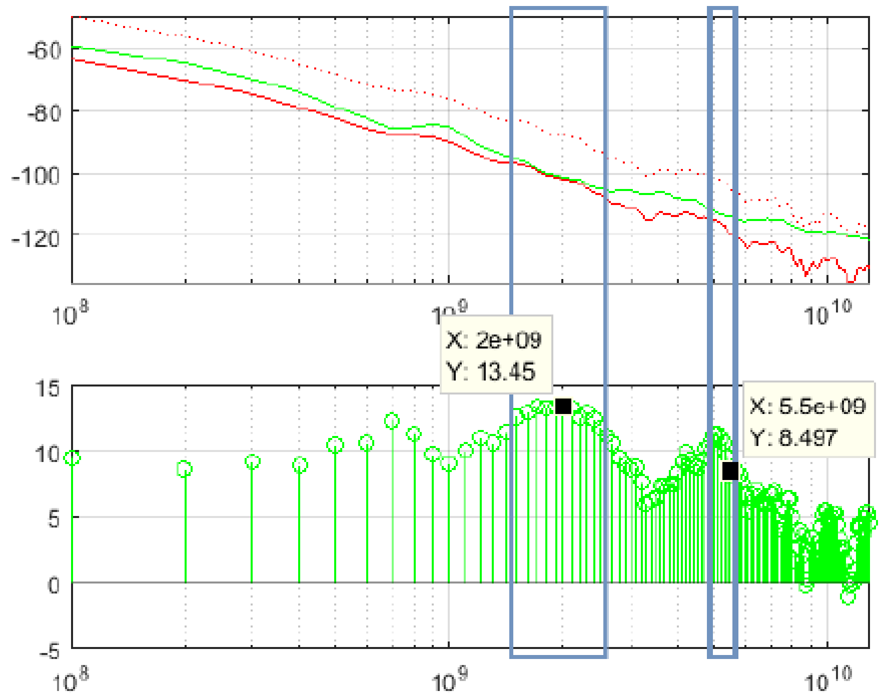
spectral peak attenuation

Numerical evaluation of the methodology in MATLAB

- Optimization in [1.5 GHz – 2.5 GHz] and [5 GHz – 5.5 GHz] frequency bands:



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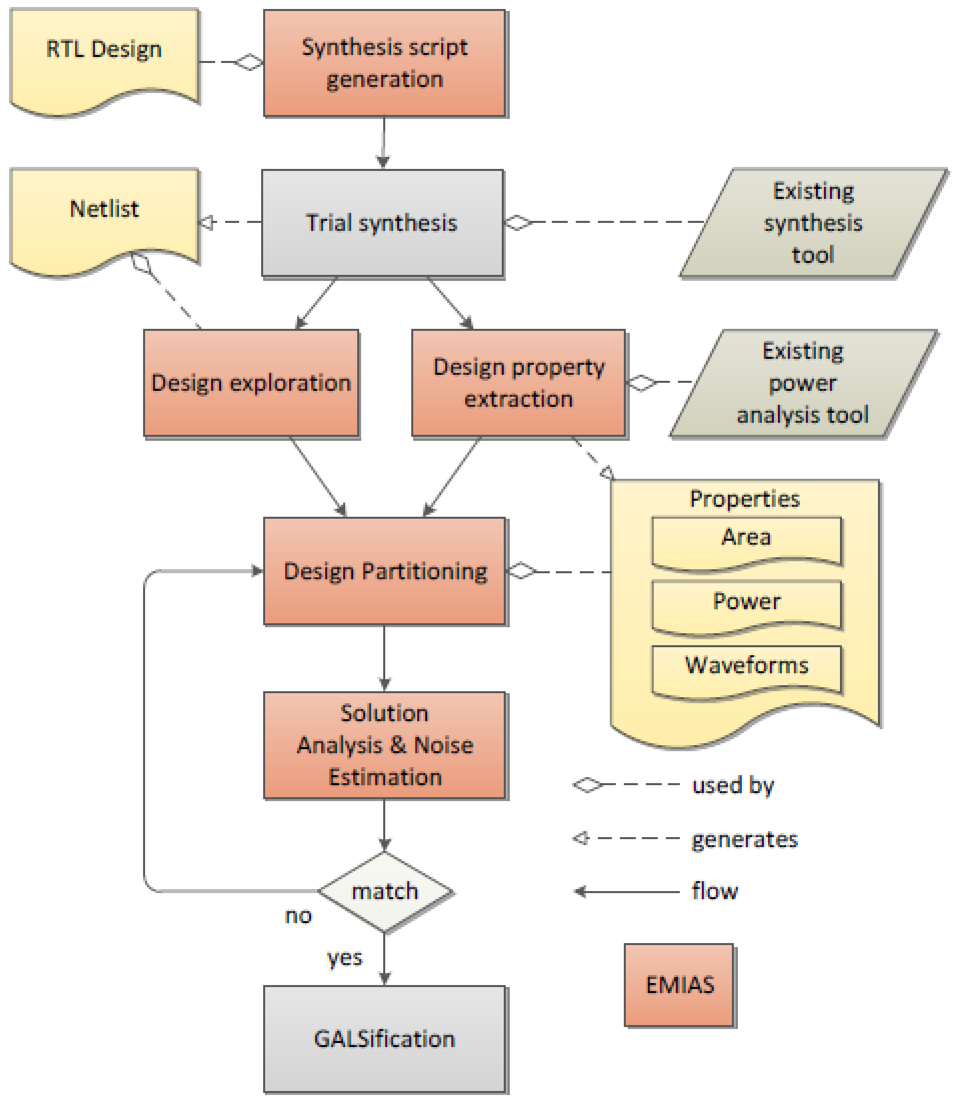
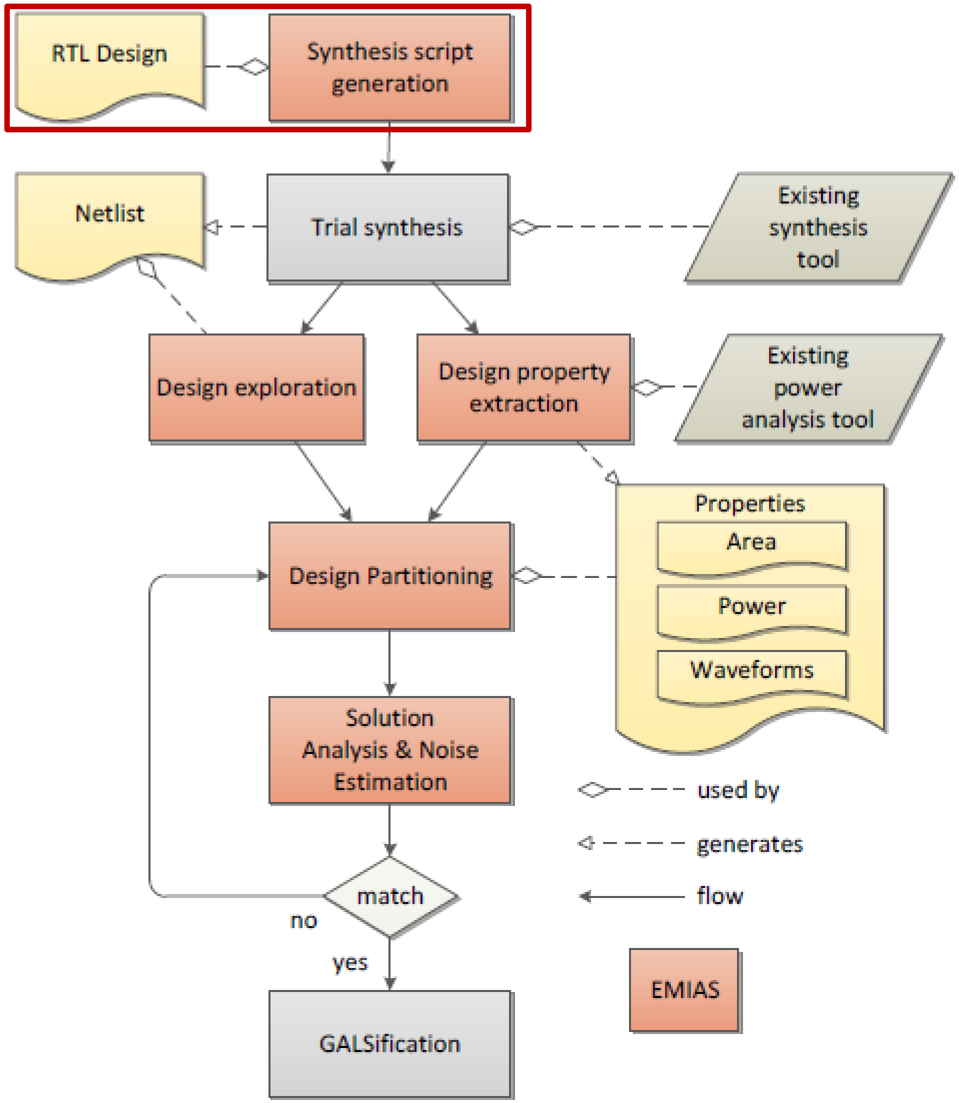
spectral peak attenuation

Agenda

EMIAS – A CAD tool for supporting the low noise design



EMIAS – A CAD tool for supporting the low noise design



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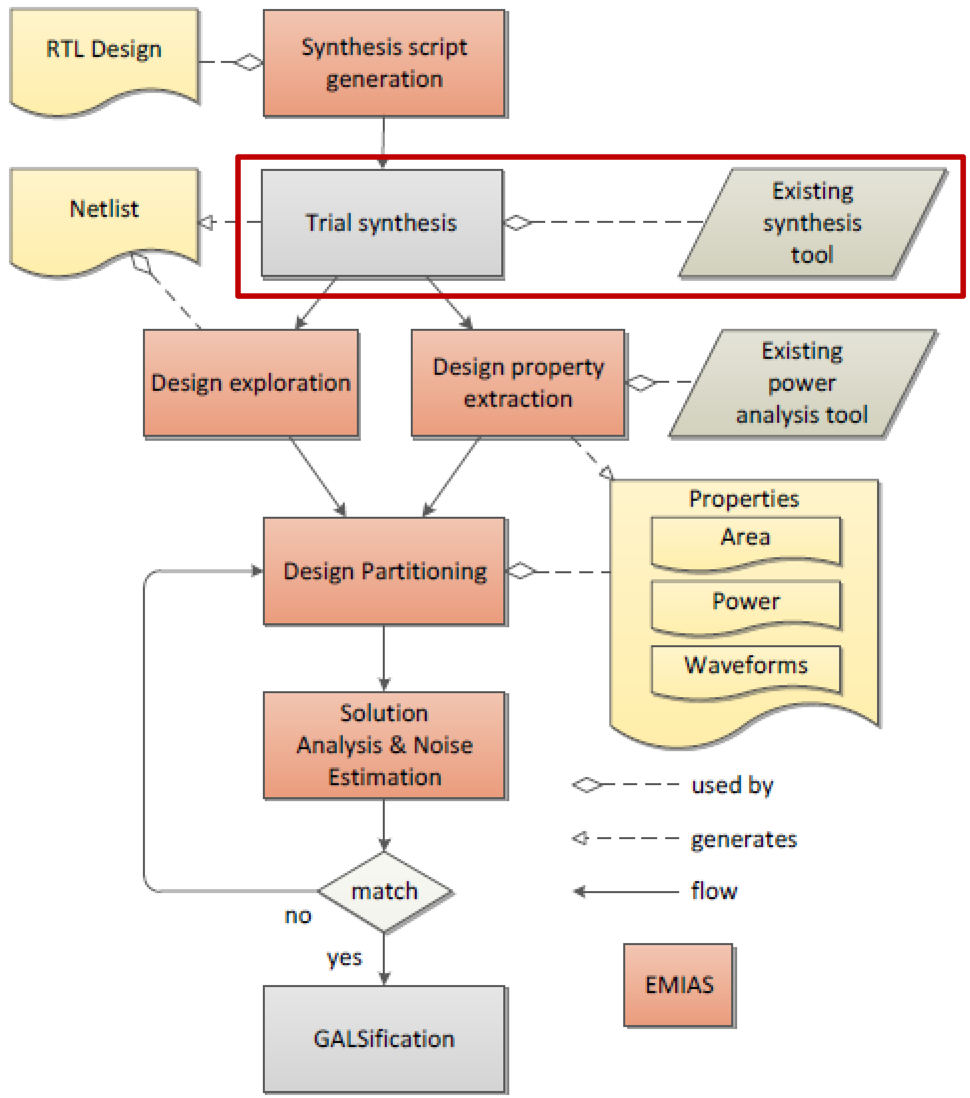

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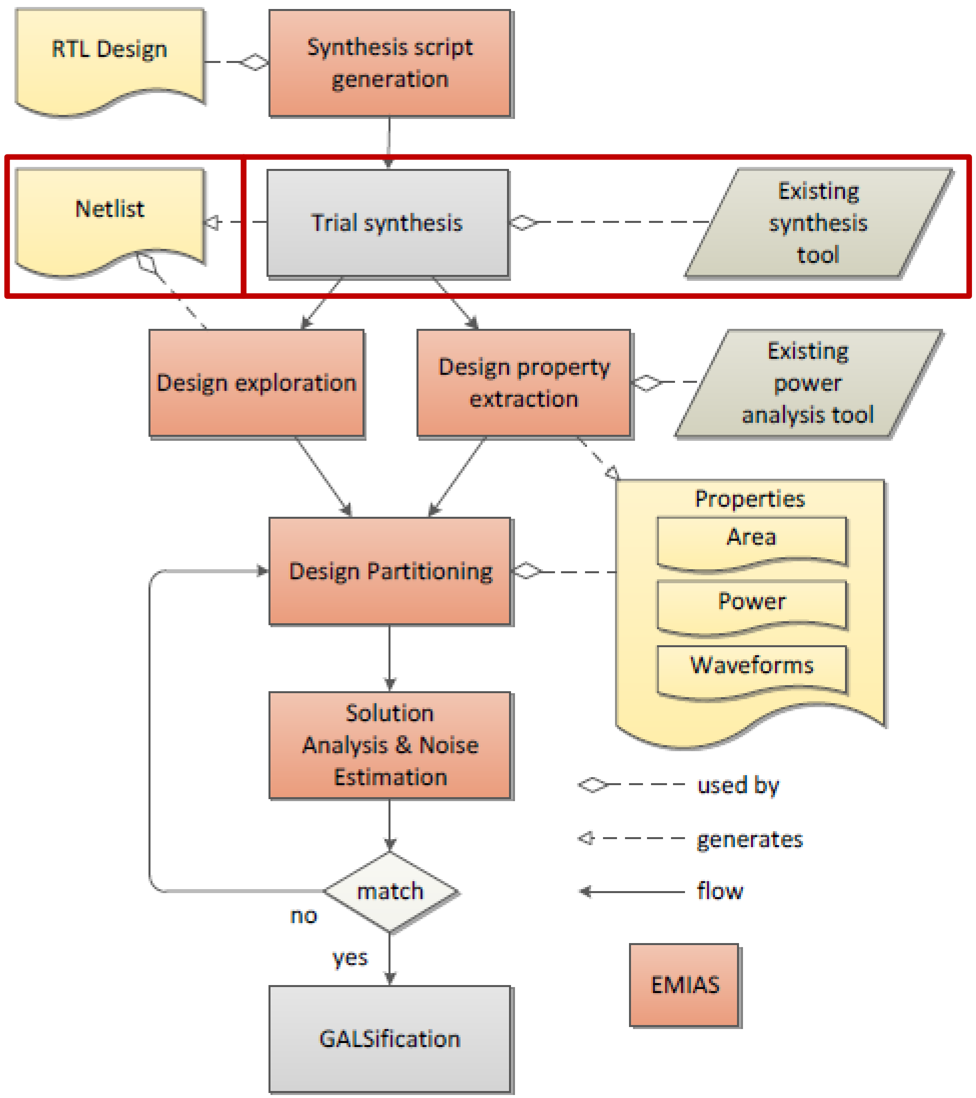

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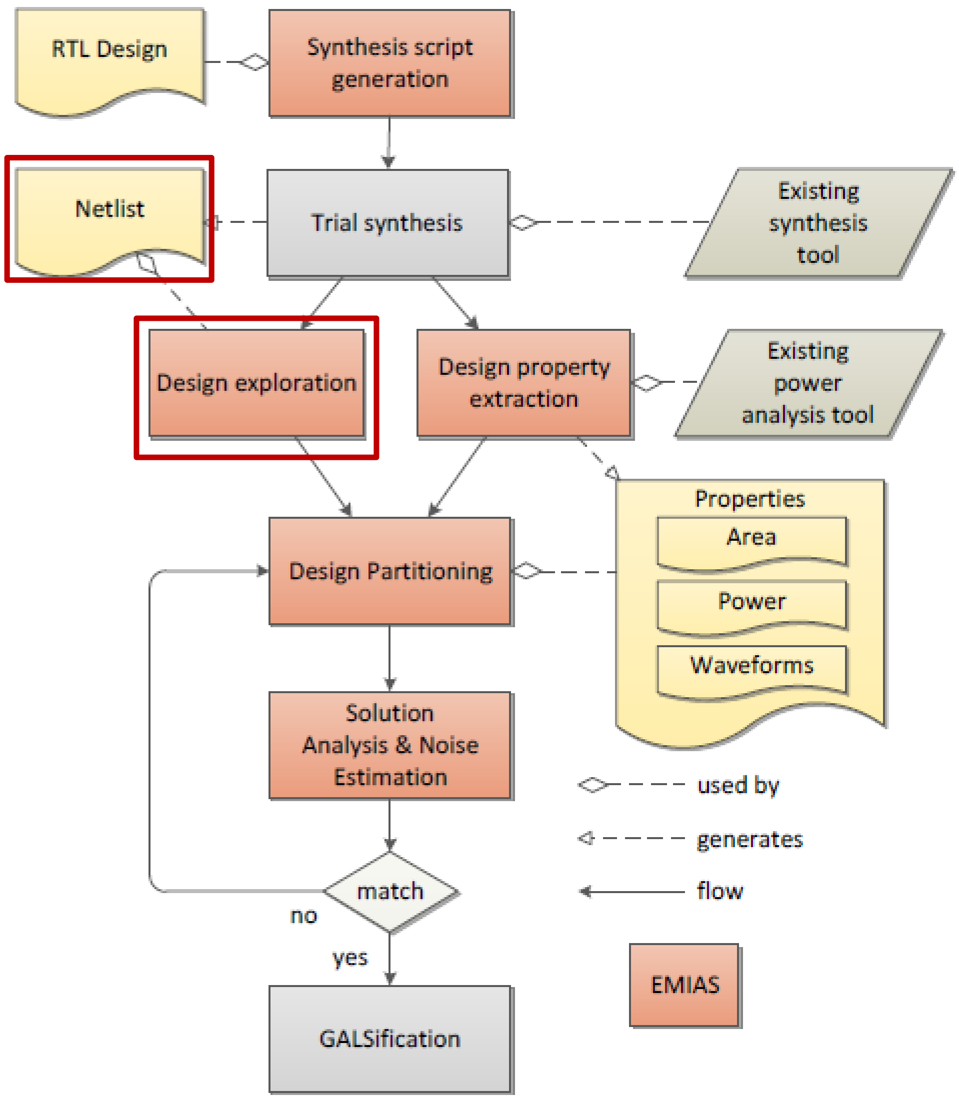

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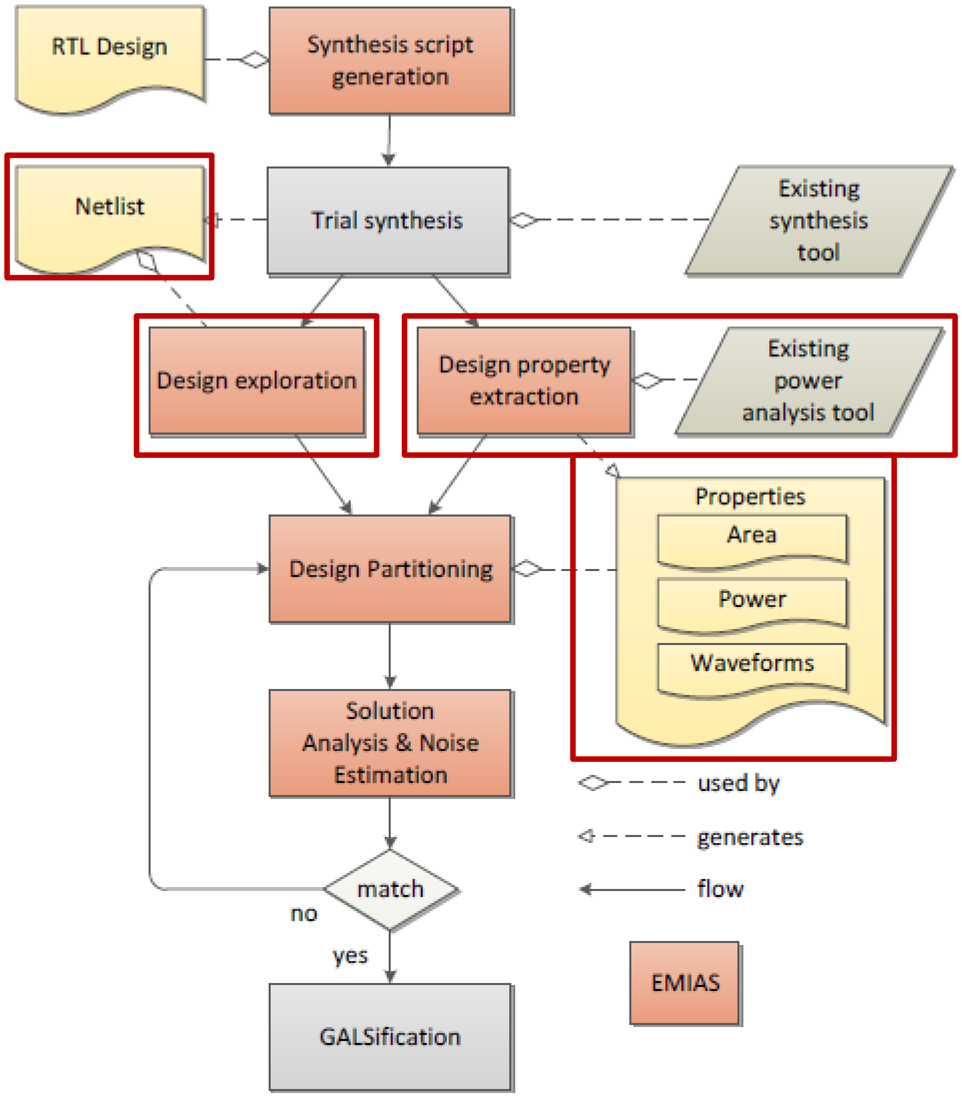

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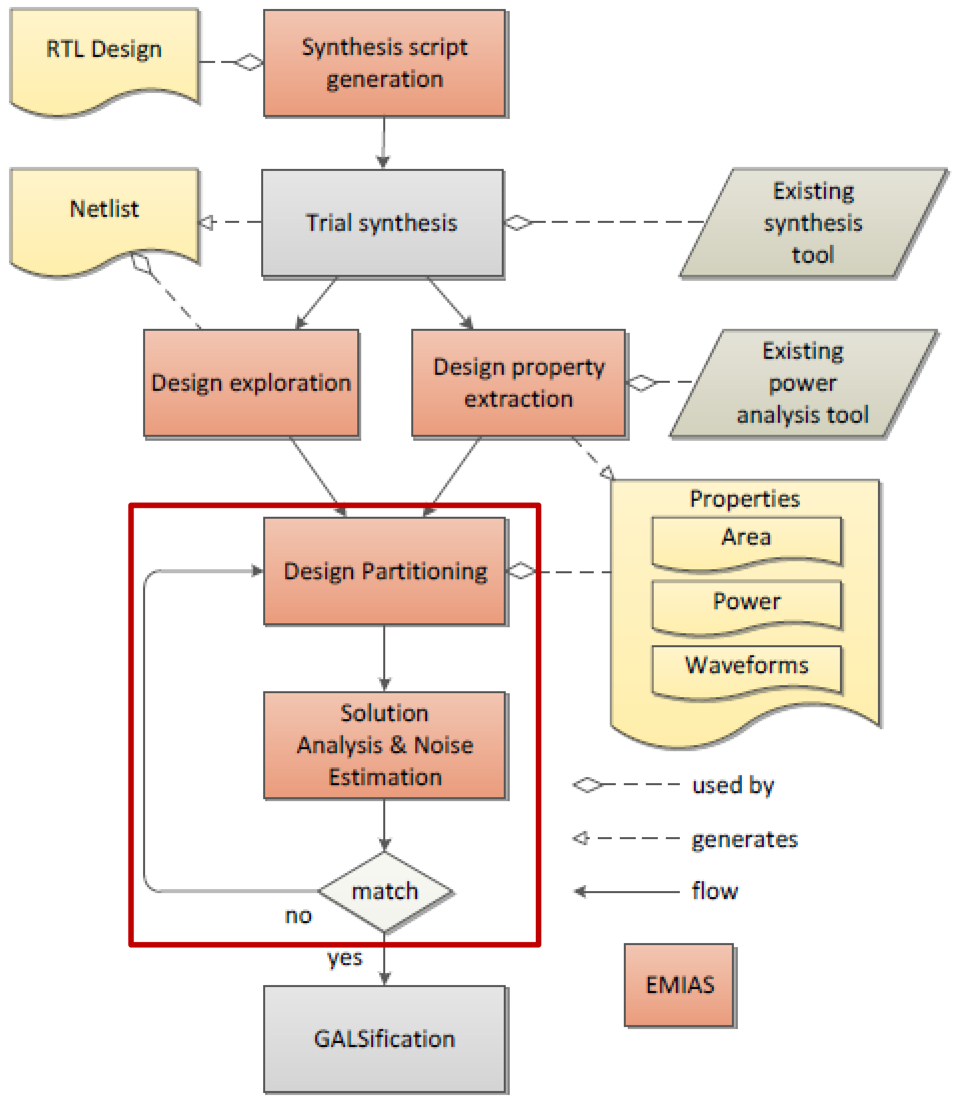
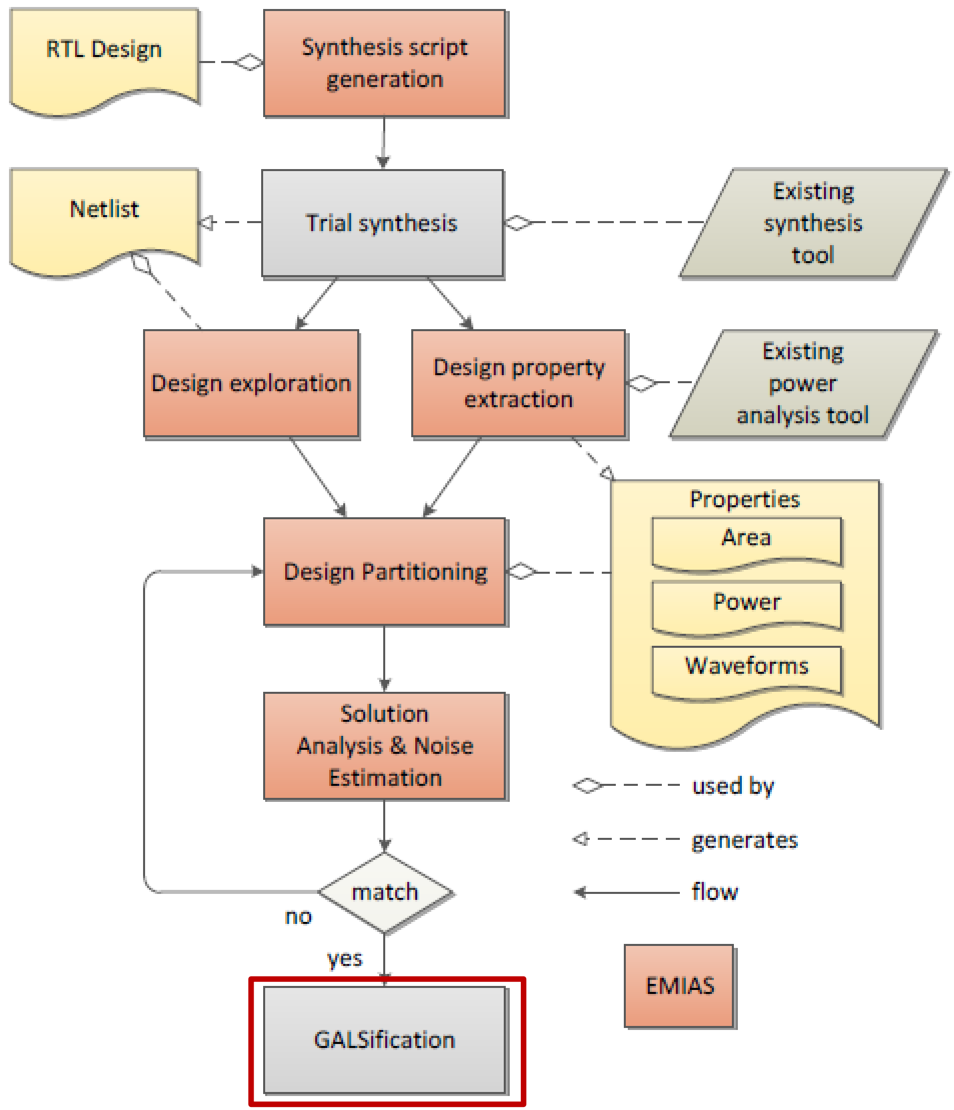


EMIAS – A CAD tool for supporting the low noise design



Application on a realistic design example

- Intended for use as a part of wireless sensor network
- LEON2 32-bit microprocessor and three accelerator cores for cryptographic operations (SHA-1, AES and ECC)
- Hierarchical netlist: 21 block
- Optimization bands:
  - The first harmonic (50 MHz) and GSM-850 band (800 MHz, 850 MHz, 900 MHz)
- 5 LSMs, frequency offsets: 2.56%, 1.26%, 0%, -1.24% and -2.44%

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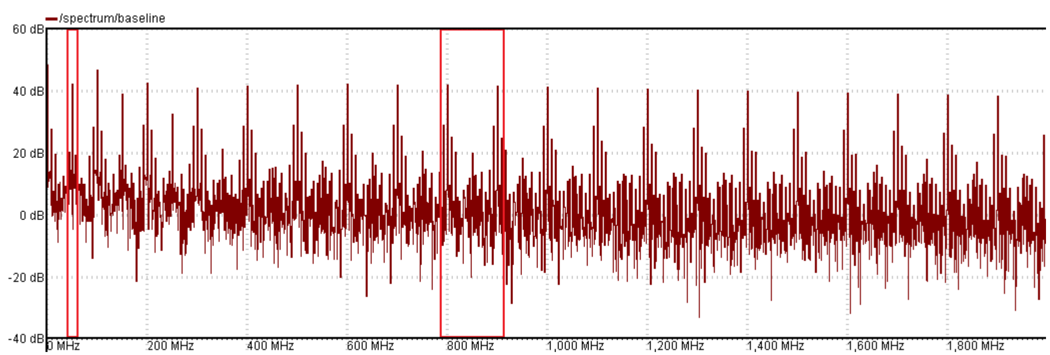
- Attenuation achieved:
  - ~7 dB for the strongest components, less for the weaker components



synchronous system

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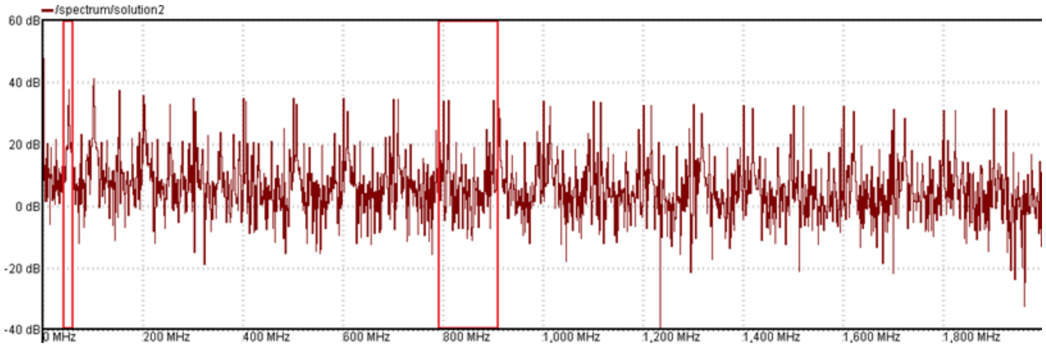

GALS system

Agenda

Conclusions and future work

- A GALS methodology for substrate noise reduction presented, based on harmonic balanced partitioning scheme
  - Use switching current profiles of design subcomponents
  - Calculate the spectra
  - Assign the design subcomponents to partitions **such that all harmonics in the targeted frequency band are as equal as possible among the partitions**

- Theoretical maximum for spectral peak attenuation:
  - $20 \log M$ for M partitions

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- A GALS methodology for substrate noise reduction presented, based on harmonic balanced partitioning scheme
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  - $20 \log M$ for M partitions

- Future work
  - Further automatization of the implemented low noise methodology

    → Automate the asynchronous wrapper integration phase
  - Fabricate a test chip to demonstrate the methodology

Thank you for your attention!

Babić, Milan

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Leibniz Association

Appendix 1: Partitioning of the design example

Table I. Harmonic peaks and harmonic power attenuations in dB

Harmonic number	1	16	17	18
Harm. frequency for the sync. system (MHz)	50	800	850	900
Synchronous system (50 MHz)	**42.26**	**41.98**	**20.16**	**41.68**
Partition 0 (51.28 MHz)	-9.42	-7.31	-9.60	-3.83
Partition 1 (50.63 MHz)	**37.74**	**34.90**	**17.72**	32.62
Partition 2 (50.00 MHz)	25.08	34.57	9.20	**34.16**
Partition 3 (49.38 MHz)	10.68	14.29	-5.47	13.81
Partition 4 (48.78 MHz)	-36.21	-6.82	-18.87	-3.29
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Harmonic peak attenuation	**4.52**	**7.08**	**2.44**	**7.52**

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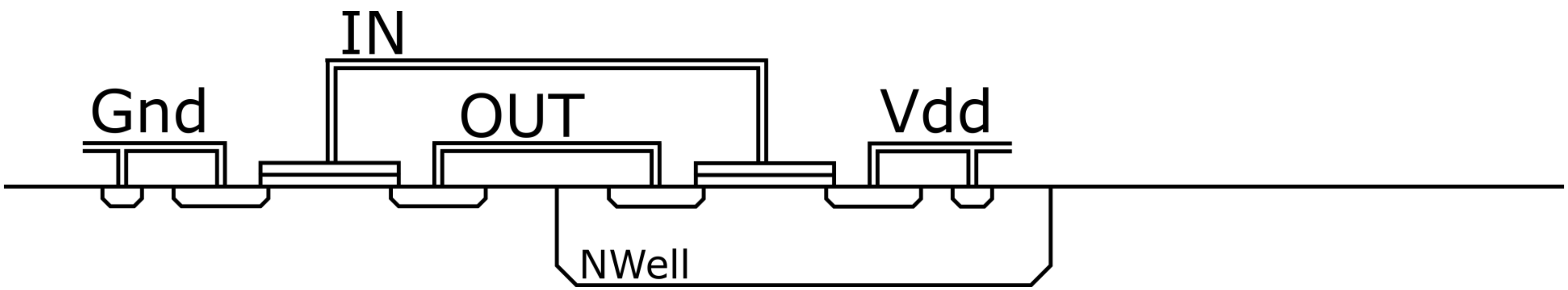
Appendix 2: Substrate noise generating mechanisms

- Ground bounce → Voltage fluctuations in the substrate (substrate noise)



Appendix 2: Substrate noise generating and injecting mechanisms

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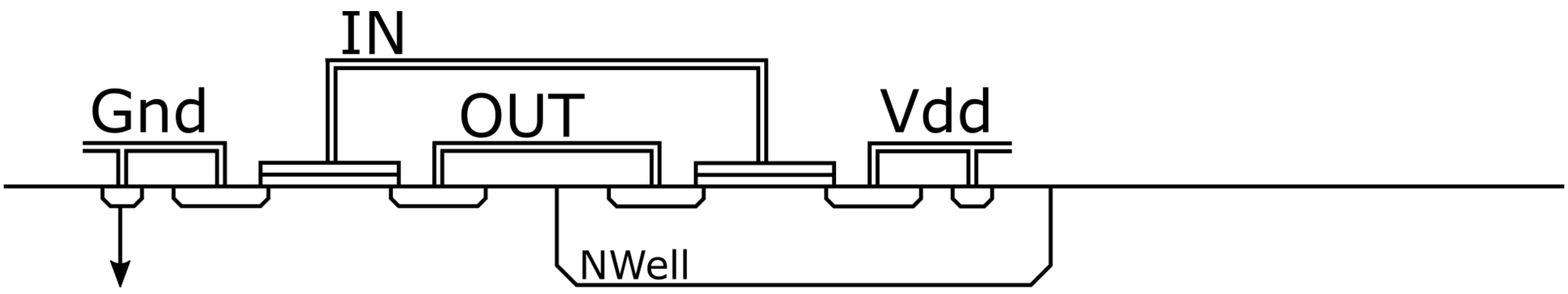

  - Direct coupling through substrate contacts

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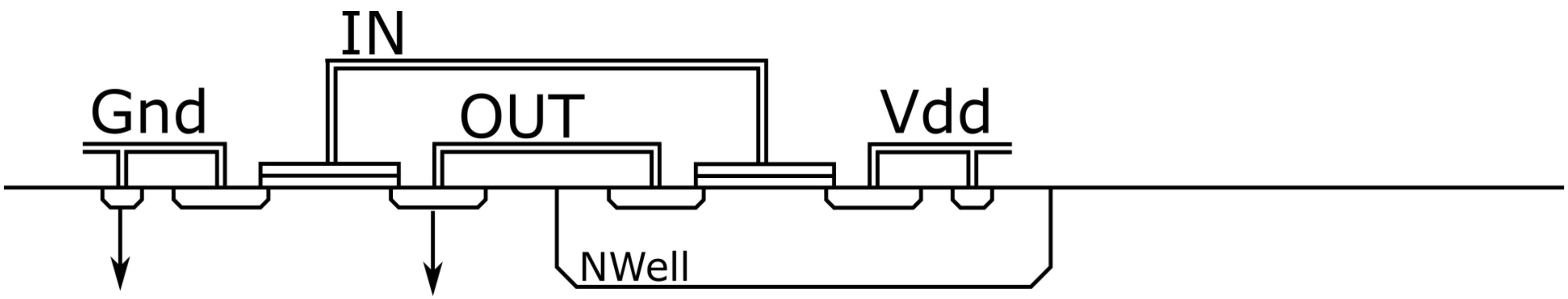

- Direct coupling through substrate contacts
- Other substrate noise sources:
  - Capacitive coupling through S/D junction capacitances

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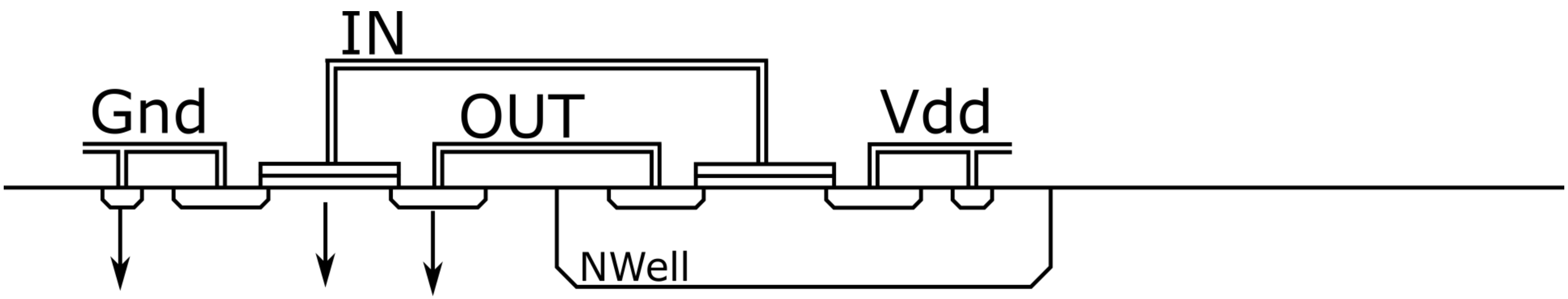

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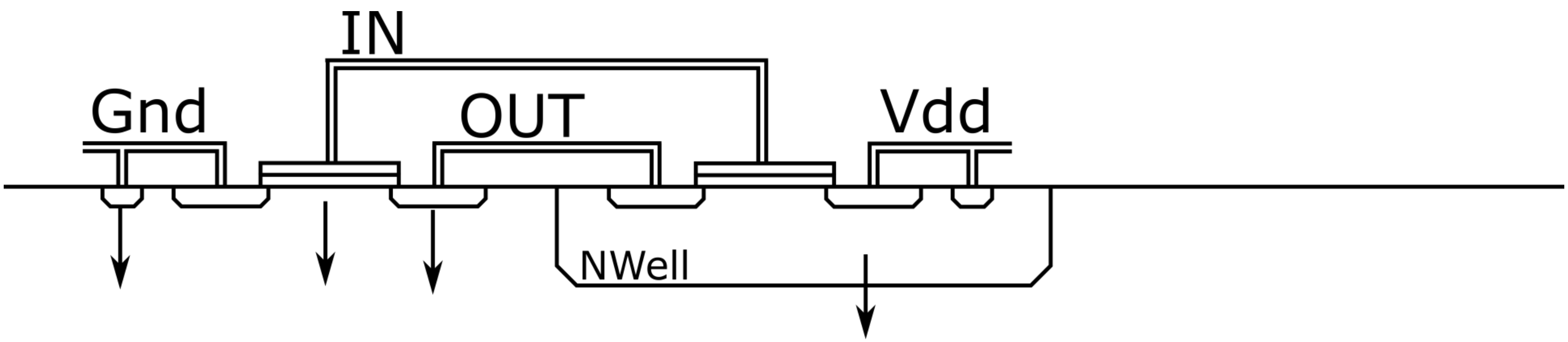

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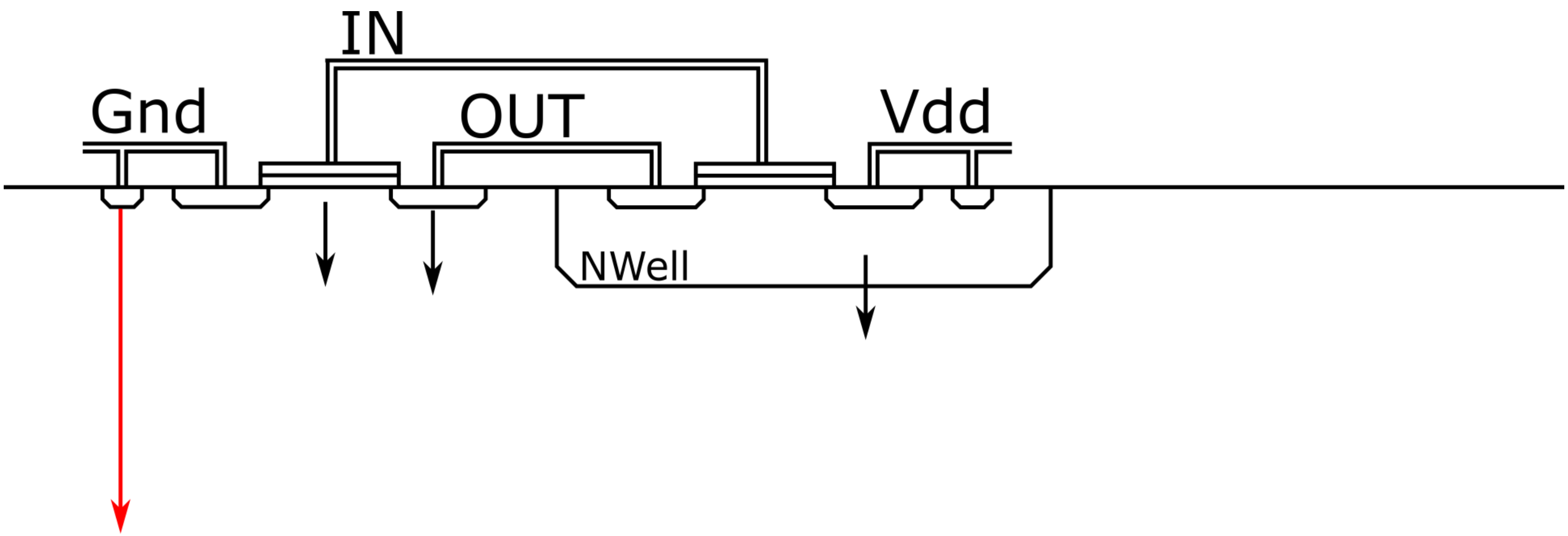

- **Direct coupling through substrate contacts → dominant coupling mechanism**
- Other substrate noise sources:
  - Capacitive coupling through S/D junction capacitances
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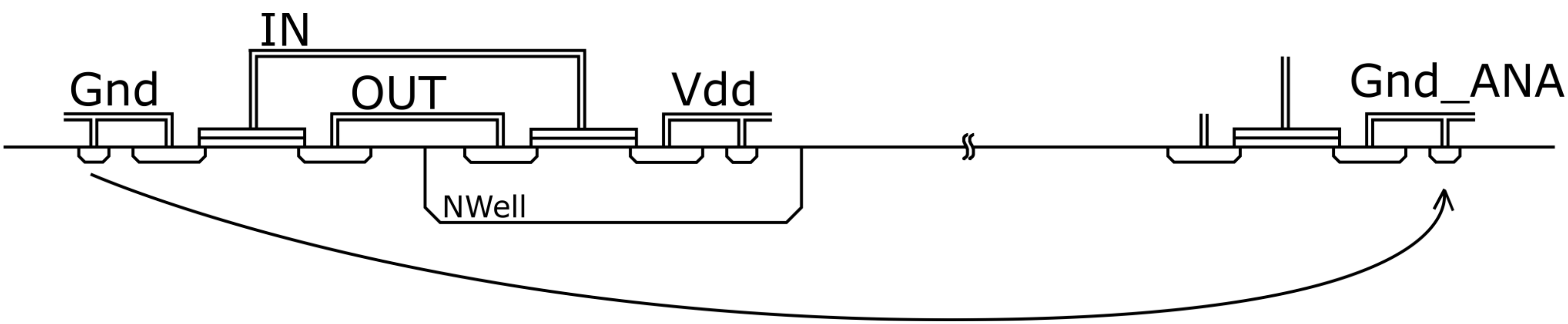
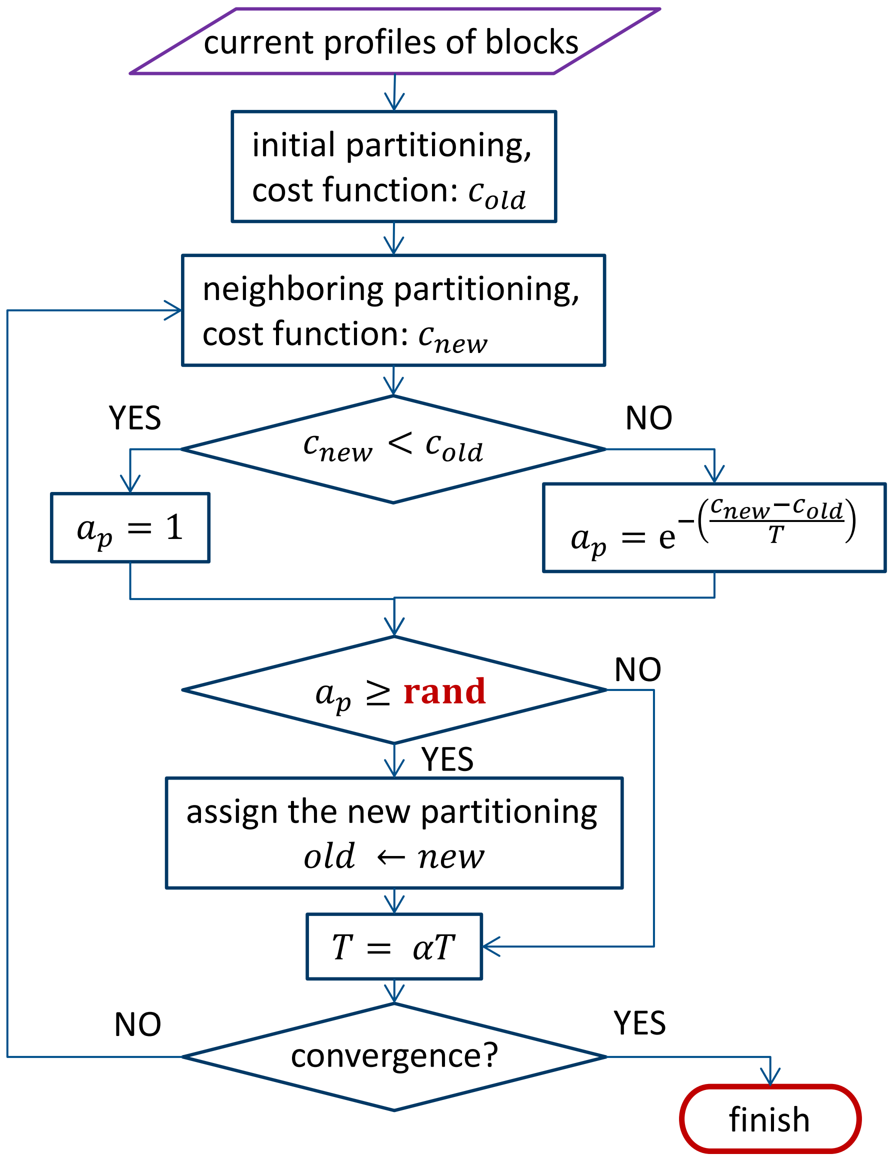


- Injection to analog circuits
  - Direct injection through substrate contacts
  - Body effect
  - Capacitive coupling through S/D junction capacitances
- This noise further propagates to the outputs of analog circuits, impacting the performance

Appendix 3: Harmonic balanced plesiochronous design in practice



Notes:

a_p – acceptance probability of the new partitioning

T – *"temperature", a parameter which gets reduced at each iteration*

$0 \leq \mathrm{rand} \leq 1$

$\alpha < 1$

Probabilistic – doesn't allways output the same combinations, especially if many combinations have a similar value of cost function

Appendix 4: Harmonic balanced plesiochronous design for substrate noise reduction

- Spectral peak attenuation:

$$i(t) = \sum_{m=1}^{M} i_m(t) \quad \Rightarrow \quad F_n\{i\} = \sum_{m=1}^{M} F_n\{i_m\} \quad \Rightarrow$$

valid for a synchronous design, approximately also valid for a plesiochronous design

$\boldsymbol{F_n\{i\}}$ – *n^{th} harmonic of the switching current spectrum for the synchronous system*

$\boldsymbol{F_n\{i_m\}}$ – *n^{th} harmonic of the switching current spectrum for the m^{th} partition of the system*

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$$i(t) = \sum_{m=1}^{M} i_m(t) \quad \Rightarrow \quad F_n\{i\} = \sum_{m=1}^{M} F_n\{i_m\}$$

$$v_{sub}(t) = \sum_{m=1}^{M} v_{subm}(t) \quad \Rightarrow \quad F_n\{v_{sub}\} = \sum_{m=1}^{M} F_n\{v_{subm}\}$$

→ *valid for a synchronous design, approximately also valid for a plesiochronous design*

$\boldsymbol{F_n\{v_{sub}\}}$ – *n^{th} harmonic of the substrate noise spectrum for the synchronous system*

$\boldsymbol{F_n\{v_{subm}\}}$ – *n^{th} harmonic of the substrate noise spectrum for the m^{th} partition of the system*

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valid for a synchronous design, approximately also valid for a plesiochronous design

$$F_n\{v_{subm}\}=H_{nm}F_n\{i_m\}$$
$$H_{n1}\approx H_{n2}\approx \ldots \approx H_{nM}\approx H_n \Rightarrow F_n\{v_{sub}\}=H_nF_n\{i\}=H_n\sum_{m=1}^{M} F_n\{i_m\}$$

$\boldsymbol{H_n}$ – *the value of substrate transfer function at the frequency of the synchronous system*

$\boldsymbol{H_{nm}}$ – *the value of substrate transfer function at the frequency of the m^{th} partition of the system*

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$$F_n\{v_{subm}\} = H_{nm} F_n\{i_m\}$$

$$H_{n1} \approx H_{n2} \approx \ldots \approx H_{nM} \approx H_n \Rightarrow F_n\{v_{sub}\} = H_n F_n\{i\} = H_n \sum_{m=1}^{M} F_n\{i_m\}$$

$$SPA_{dB} = 20 \log \frac{|F_n\{v_{sub}\}|}{\max\{|F_n\{v_{subm}\}|\}}$$

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- Spectral peak attenuation:

$$i(t) = \sum_{m=1}^{M} i_m(t) \Rightarrow F_n\{i\} = \sum_{m=1}^{M} F_n\{i_m\}$$

$$v_{sub}(t) = \sum_{m=1}^{M} v_{subm}(t) \Rightarrow F_n\{v_{sub}\} = \sum_{m=1}^{M} F_n\{v_{subm}\}$$

valid for a synchronous design, approximately also valid for a plesiochronous design

$$F_n\{v_{subm}\} = H_{nm} F_n\{i_m\}$$
$$H_{n1} \approx H_{n2} \approx \ldots \approx H_{nM} \approx H_n \Rightarrow F_n\{v_{sub}\} = H_n F_n\{i\} = H_n \sum_{m=1}^{M} F_n\{i_m\}$$

$$SPA_{dB} = 20\log \frac{|F_n\{v_{sub}\}|}{\max\{|F_n\{v_{subm}\}|\}} \approx 20\log \frac{|F_n\{i\}|}{\max\{|F_n\{i_m\}|\}}$$

Appendix 4: Harmonic balanced plesiochronous design for substrate noise reduction

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Appendix 4: Harmonic balanced plesiochronous design for substrate noise reduction

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- Optimal partitioning:
  - Group the blocks into partitions so that the harmonics aimed for reduction be the same for each of the partitions

$$F_n\{i_1\} = F_n\{i_2\} = \ldots = F_n\{i_M\} = \frac{F_n\{i\}}{M} \Rightarrow \max\{SPA_{dB}\} = 20\log M$$

Appendix 4: Harmonic balanced plesiochronous design for substrate noise reduction

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