Low Power QDI Asynchronous FFT

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Motivation

- Extreme long battery life is crucial for M2M communication
- Must push innovation in low-power communication
- FFT is a common IP block that is computationally and memory intensive

FFT

- DFT: $$X[k] = \sum_{n=0}^{N-1} x[n]\, e^{-j\frac{2\pi k}{N}n}, \quad k = 0, 1, \ldots., N-1$$

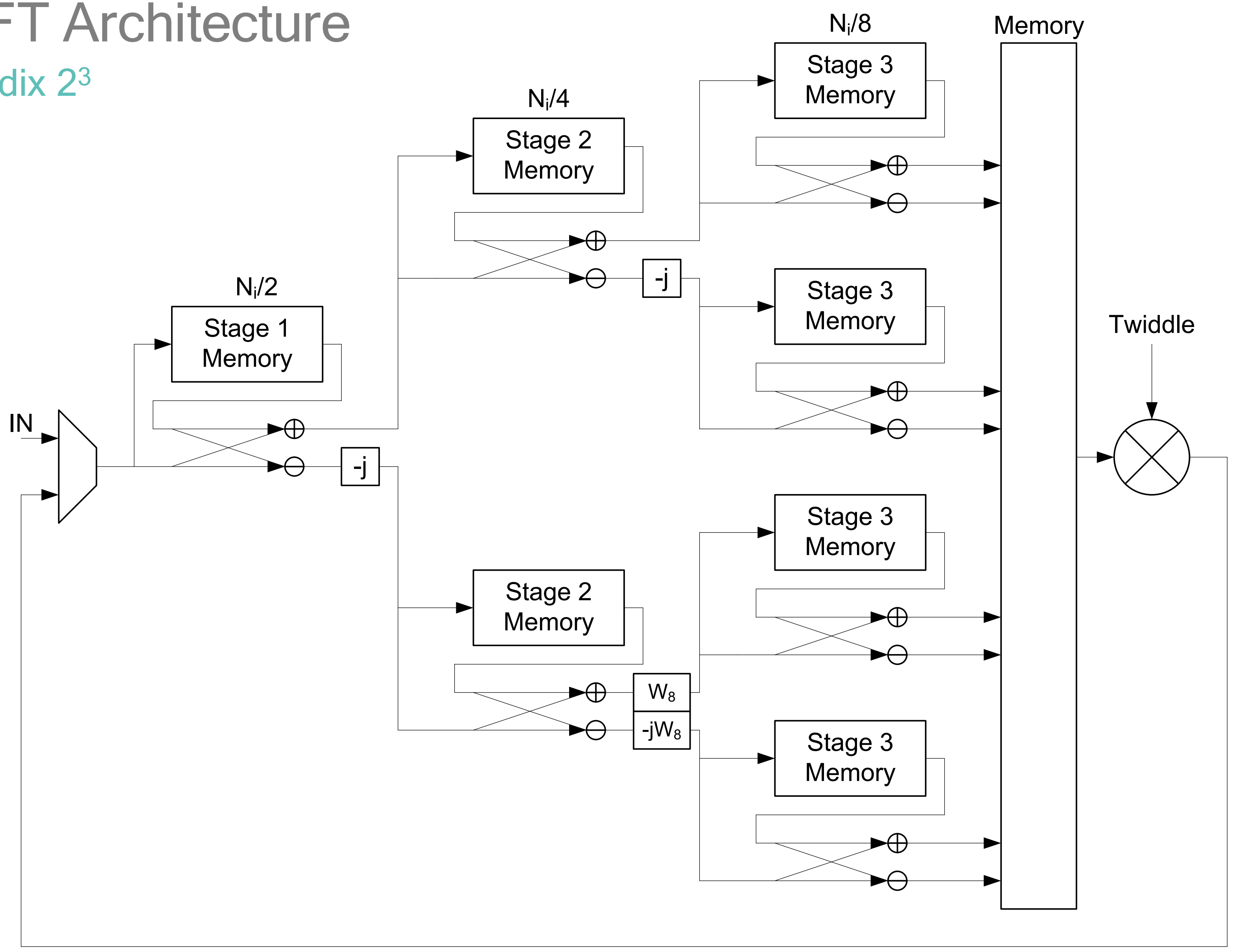
- FFT: O(N log(N))

- Implementation options:
  - Algorithm level: Radix, DIT/DIF, number representation
  - Circuit level: Twiddle multiplication, CORDIC rotation, multi-rate clocking, etc

- Reference sync version:
  - Radix 2^3
  - Decimation in frequency (DIF)
  - 16-bit real, 16-bit imaginary
  - Twiddle multiplication: (a+bj)*(c+dj) = (ac-bd) + (ad+bc)j

FFT Architecture

Radix 2^3



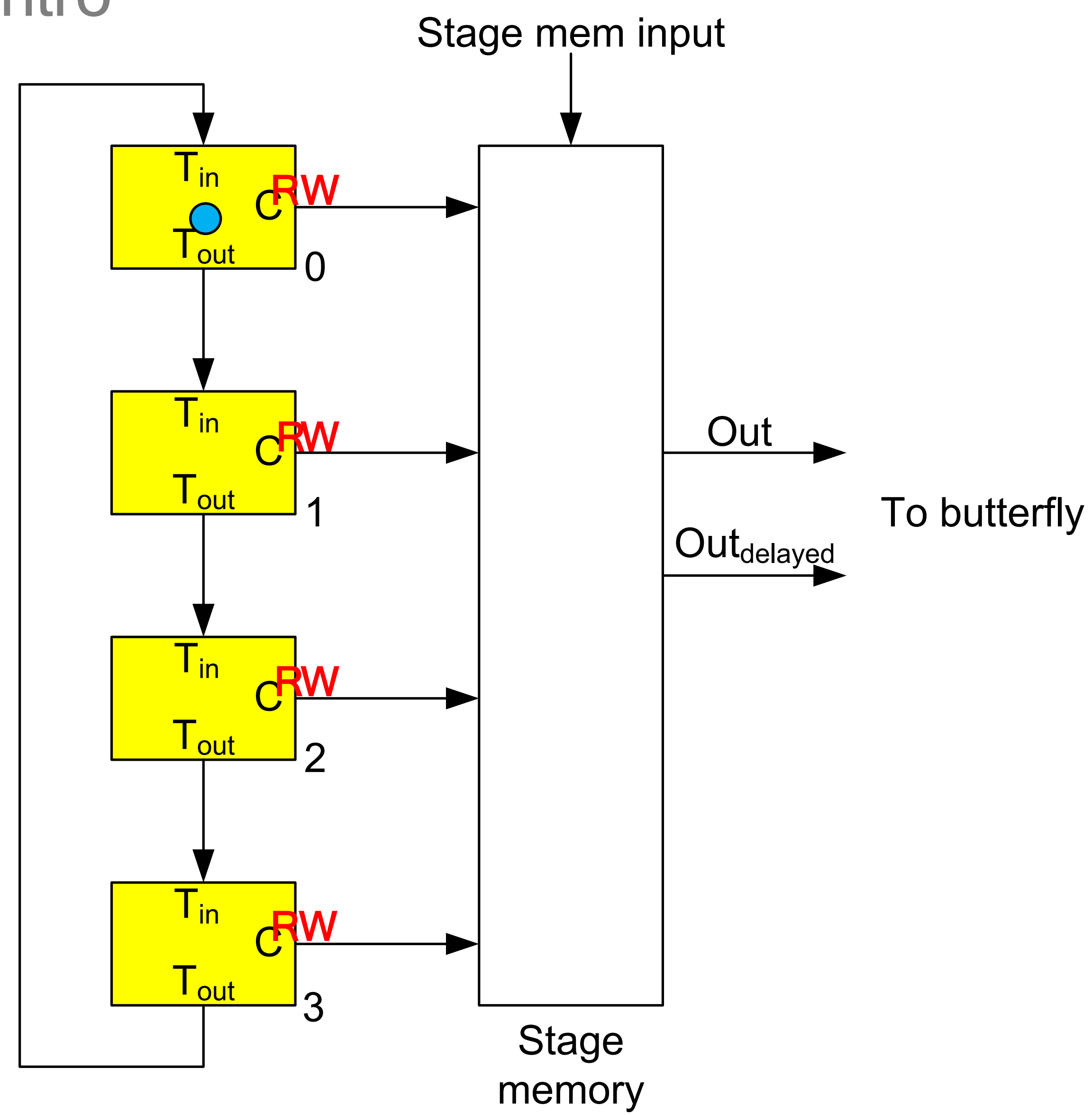
Async FFT

- QDI
- Micro-architecture optimizations highlights:
  - Token ring memory controls
  - CORDIC twiddle multiplication

Token-Ring Memory Intro

Example:

- 1st stage of 8-pt FFT
- 1-D ring

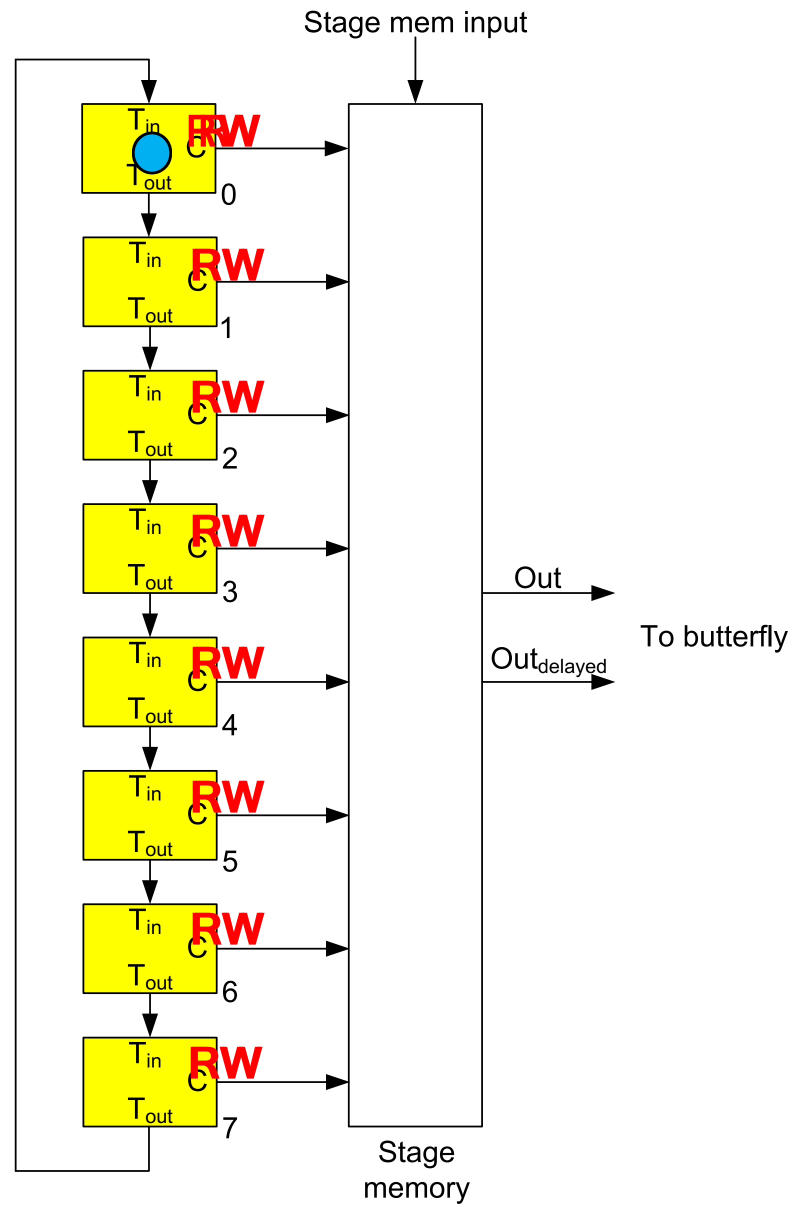


Token-Ring Controls

16-point FFT

1st stage example

- 2 passes, need 2-D ring
- 1st pass: store 8, read 8, once
- 2nd pass: store 1, read 1, 8 times
- Token ring keeps track of pattern



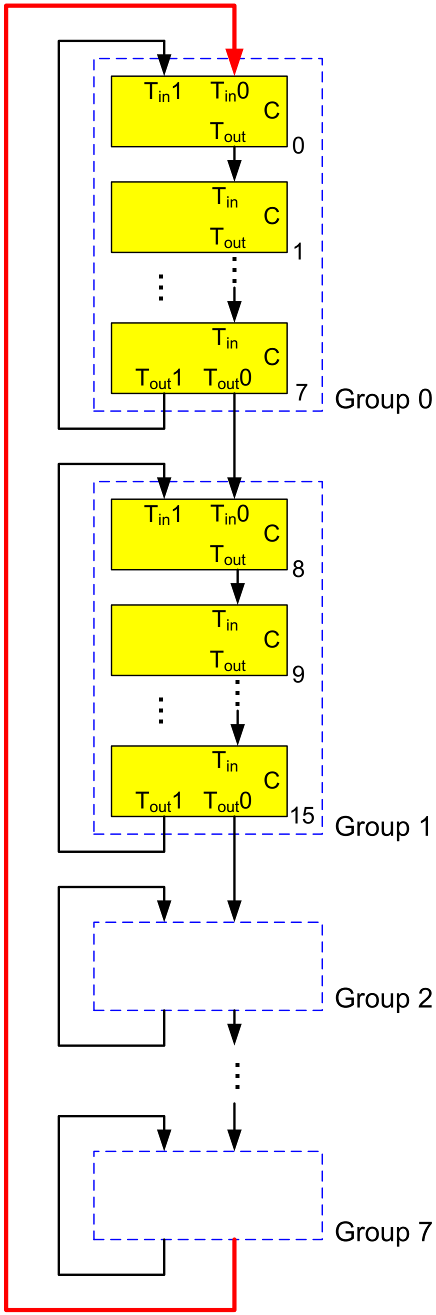
Token-Ring Controls

128-point FFT

1st stage example

- 3 passes, need 3-D ring, with 8 groups of 8
- 1^{st} pass: store 64, read 64, once
- 2^{nd} pass: store 8, read 8, 8 times
- 3^{rd} pass: store 1, read 1, 64 times

Token rings provide controls for memory read/write, automatic back-pressure, counting and addressing



CORDIC Rotation Intro

- Twiddle ($e^{-j(2\pi kn/N)}$) multiplication = rotation by angle -(2πkn/N)
- Pipelined vs iterative
- Performance, area, clock cycles

$$x_{i+1} = x_i - y_i \times d_i \times 2^{-i}$$

$$y_{i+1} = y_i + x_i \times d_i \times 2^{-i}$$

$$z_{i+1} = z_i - d_i \times \arctan 2^{-i}$$

$$d_i = \begin{cases} -1, & z_i < 0 \\ 1, & z_i \geq 0 \end{cases}$$

$$x_0 = x_{in}$$

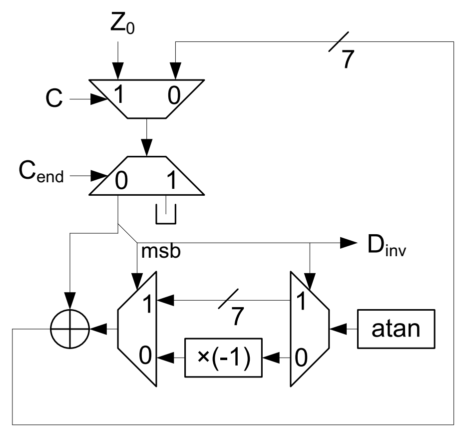
$$y_0 = y_{in}$$

$$z_0 = rotation\ angle$$

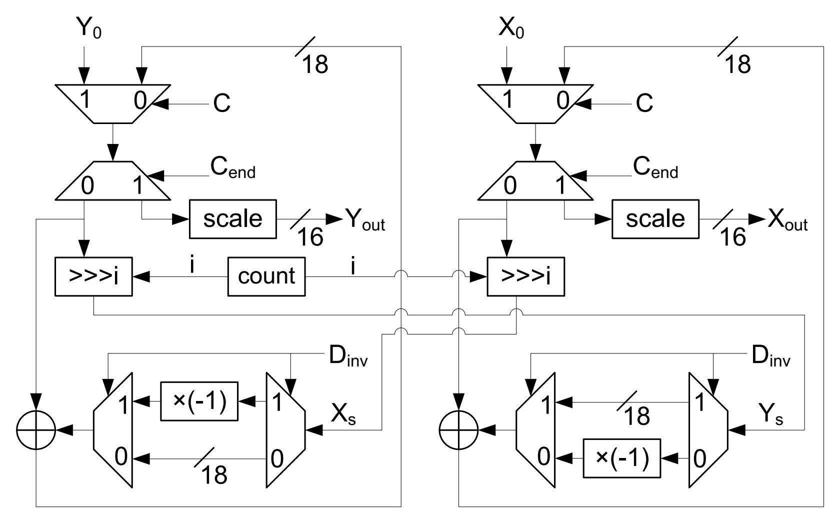
Chose iterative architecture

Asynchronous CORDIC Engine

- 6 iterations
- Bypass CORDIC for 0 degrees
  - About 37% of the time in 128-point FFT
  - Increased performance, reduced power



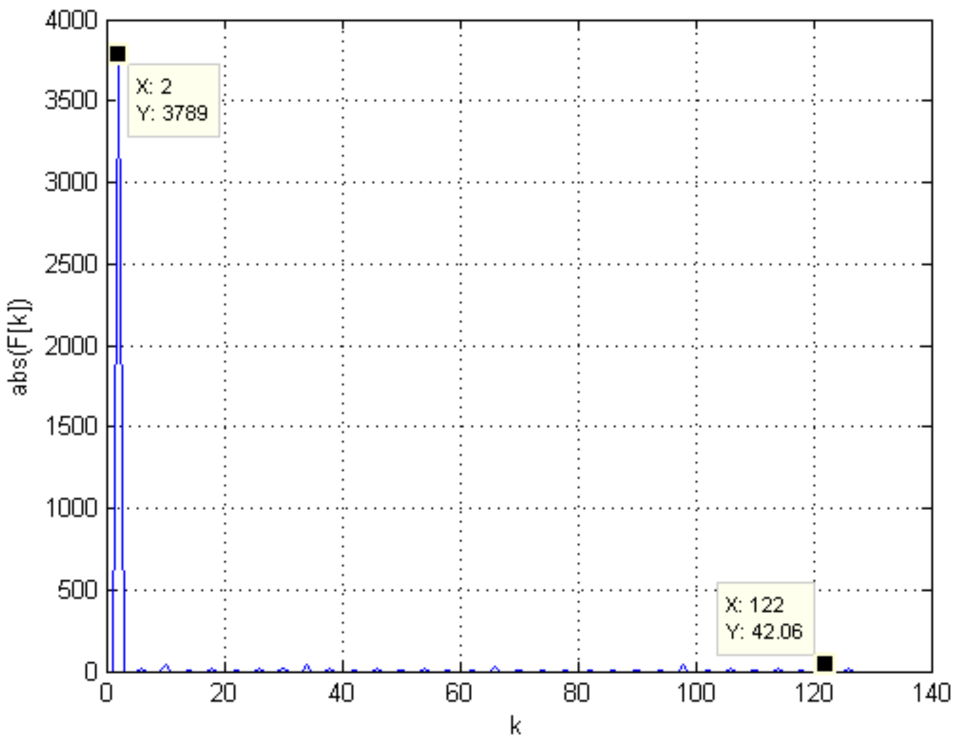
C=*[1,0,0,0,0,0,0]
C_{end}=*[0,0,0,0,0,0,1]



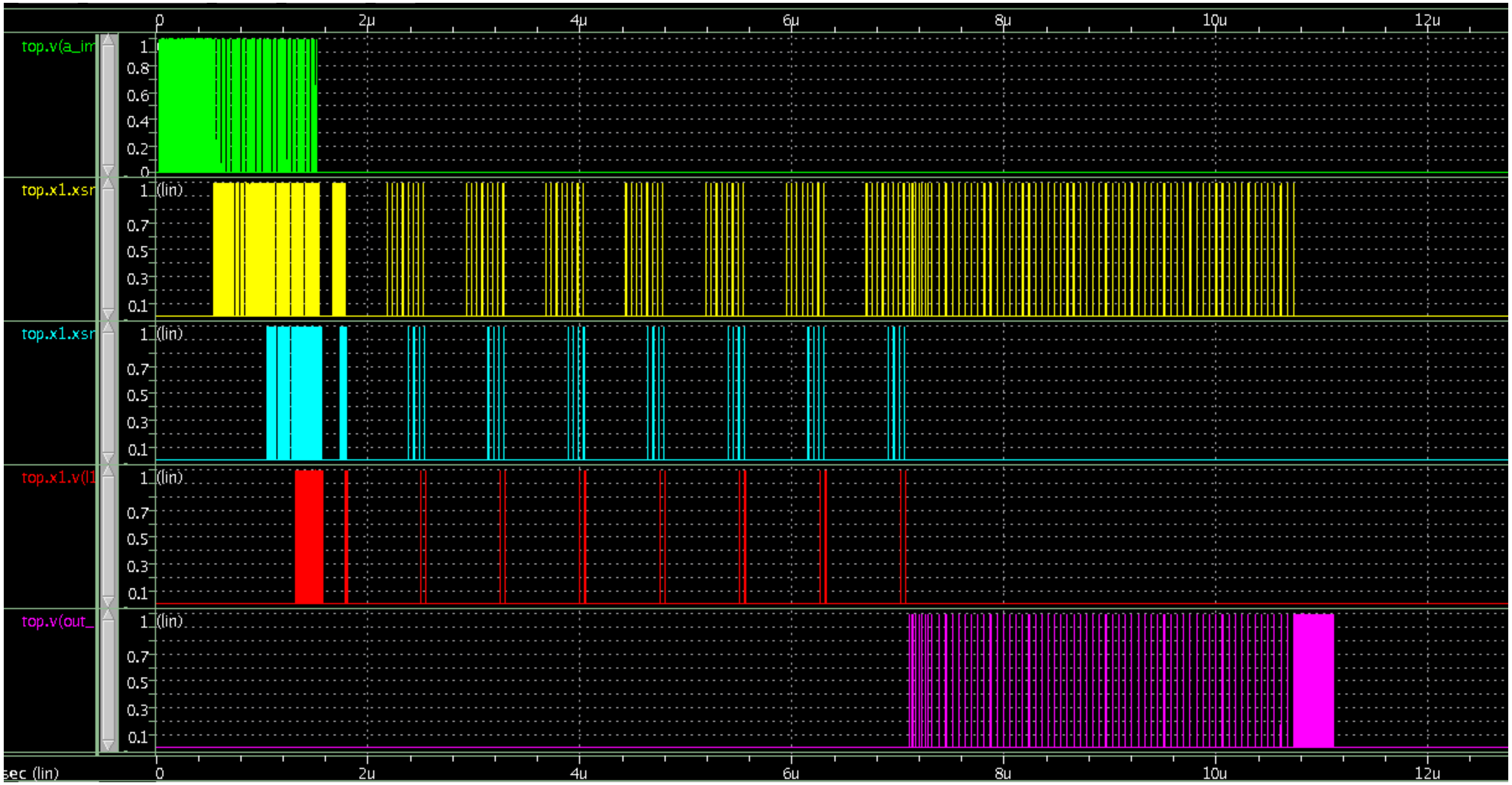
Ramps up performance to cycle through iterations without being constrained by system clock

Results - FFT Plot

- CHP ⟶ production rules ⟶ transistor-level (Spice) netlist
- Sinusoid input, negligible difference compared to result from Matlab's native FFT function



Results – Spice Waveforms



Inputs

1st stage

2nd stage

3rd stage

Outputs

Results - Power

- 65nm technology
- Vdd=1V
- 10 MHz data rate

Subsystems	Energy (nJ)
Memories, controls, butterflies, others	3.1
CORDIC	2.8
Total	**5.9**

Results – Comparison

	This Work	Sync (Chip)*	[1]	[2]
Tech	65 nm	65 nm	65 nm	0.35 µm
Voltage	1.0 V	1.0 V	0.3 V	1.1 V
N-point	128	128	128	128
Data rate	10 MHz	10 MHz	-	16 kHz
Energy	5.9 nJ	205 nJ	31 nJ	120 nJ

* Normalized to same data rate and FFT length

[1] K.-S. Chong, J. Chang, I. Ebong, Y. Yilmaz, and P. Mazumder, “Comparison of FFT/IFFT Designs Utilizing Different Low Power Techniques,” in Electronic System Design (ISED), 2012 International Symposium.

[2] K.-S. Chong, B.-H. Gwee, and J. S. Chang, “Energy-Efficient Synchronous-Logic and Asynchronous-Logic FFT/IFFT Processors,”, IEEE Journal of Solid-State Circuits, 2007.

Summary

- Low power clockless FFT design
  - Same design concepts can be extended to high performance systems
  - Can lower supply voltage further for near-threshold computing
- Simple, fast token rings memory controls
- Small, fast CORDIC engine

Acknowledgment

- Rajit Manohar for async CAD tools

Thank you

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