

FROM RESEARCH TO INDUSTRY

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Ultra Low Power and low cost Asynchronous Service Network Architecture for Adaptive Blocks Reconfiguration in an IoT Wireless Sensor Node Circuit

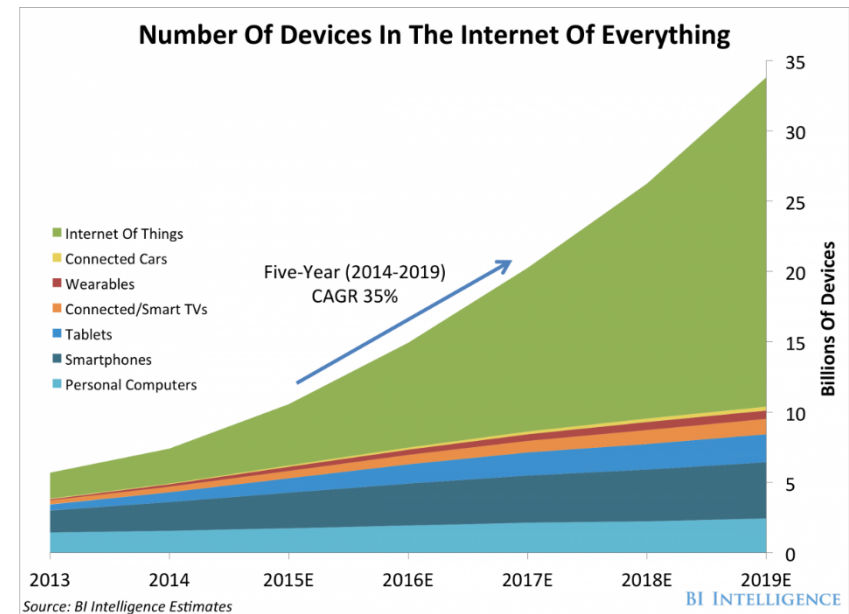
ASYNC 2016

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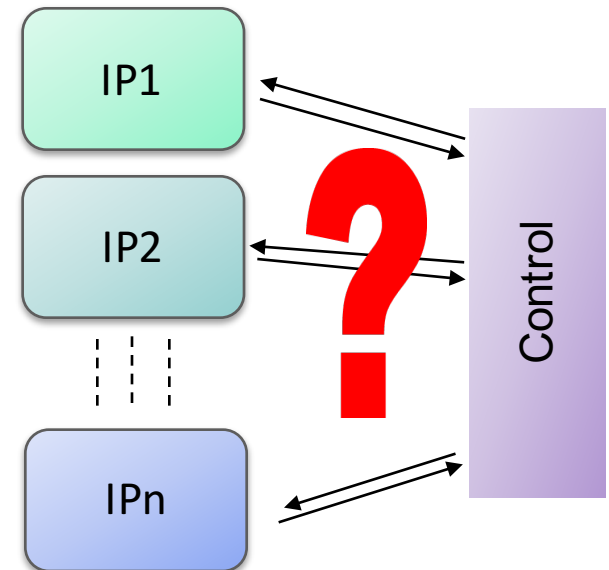
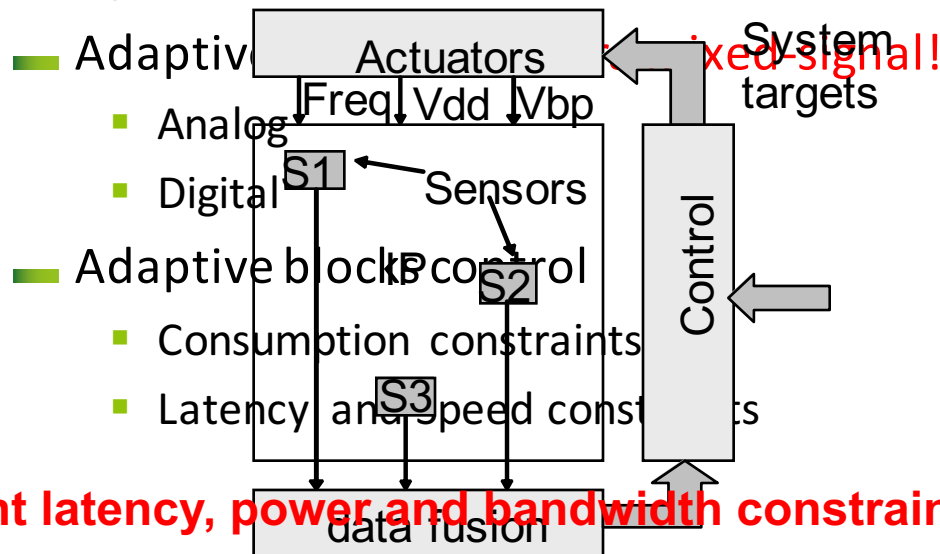
- **30 to 50 billions** of smart-objects by 2020 (The Economist & BI)
- Many applications to address **new challenges**
 - 70 % of the World's population in cities by 2050 ➔ **smart-building & transport**
 - 33 % of the World's population over 65 years old by 2050 ➔ **smart-health**
- **Why low-power ?**
 - Global Energy Impact
 - Convenience (all-day battery life)
 - Small form factor (in-body implants)
 - Maintenance-free (wide deployment)



Adaptativity for Low Energy in WSN

- Low power in WSN is an important system requirement
- Adaptativity in WSN for low energy
 - Tracking the Optimum Energy Point
 - Adaptativity to on-going application requirements
 - Adaptativity to on-going environment

Adaptive blocks control



Different latency, power and bandwidth constraints What interconnection network ?

SoA: usual communication networks

	Bus	Topology	Frame		Arbitration
			Data_bus	Address_bus	
CoreConnect	PLB	Hierarchical bus	32/64/128/256	32	Priority
	OPB	Hierarchical bus	32	32	Priority
	DCR	Daisy chain	32	10	Priority
AMBA	AHB	Hierarchical bus	32/64/128/256	32	Application dependent
	APB	Hierarchical bus	32/64/128/256	32	X

■ AMBA (ARM)

- Frame adapted for large data

■ CoreConnect:

- DCR: used for configuration purposes
- Can only reconfigure digital blocks

Problem: networks designed for multi-core communication

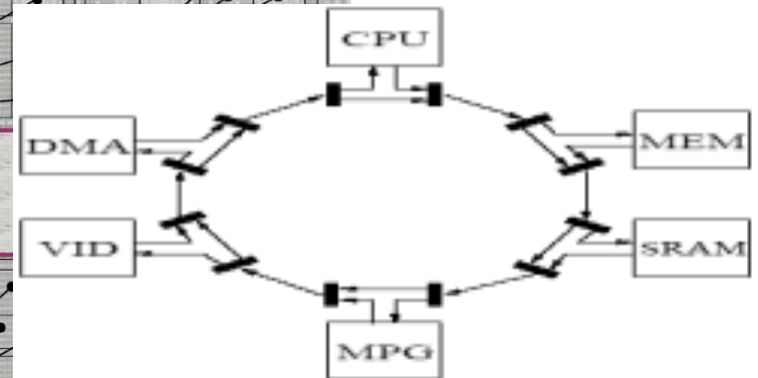
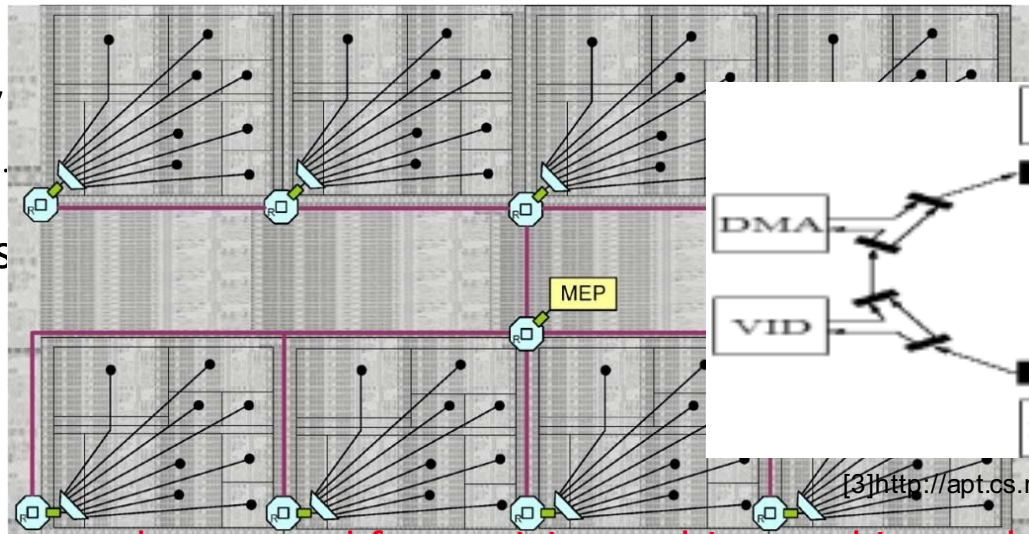
- Too high of a throughput
- DCR is oversized

■ MNoC (Monitoring Network on Chip)

- Packetization of data into flits => routing thanks to LUTs => depacketisation
- Use of 2 channels: priority and normal channel

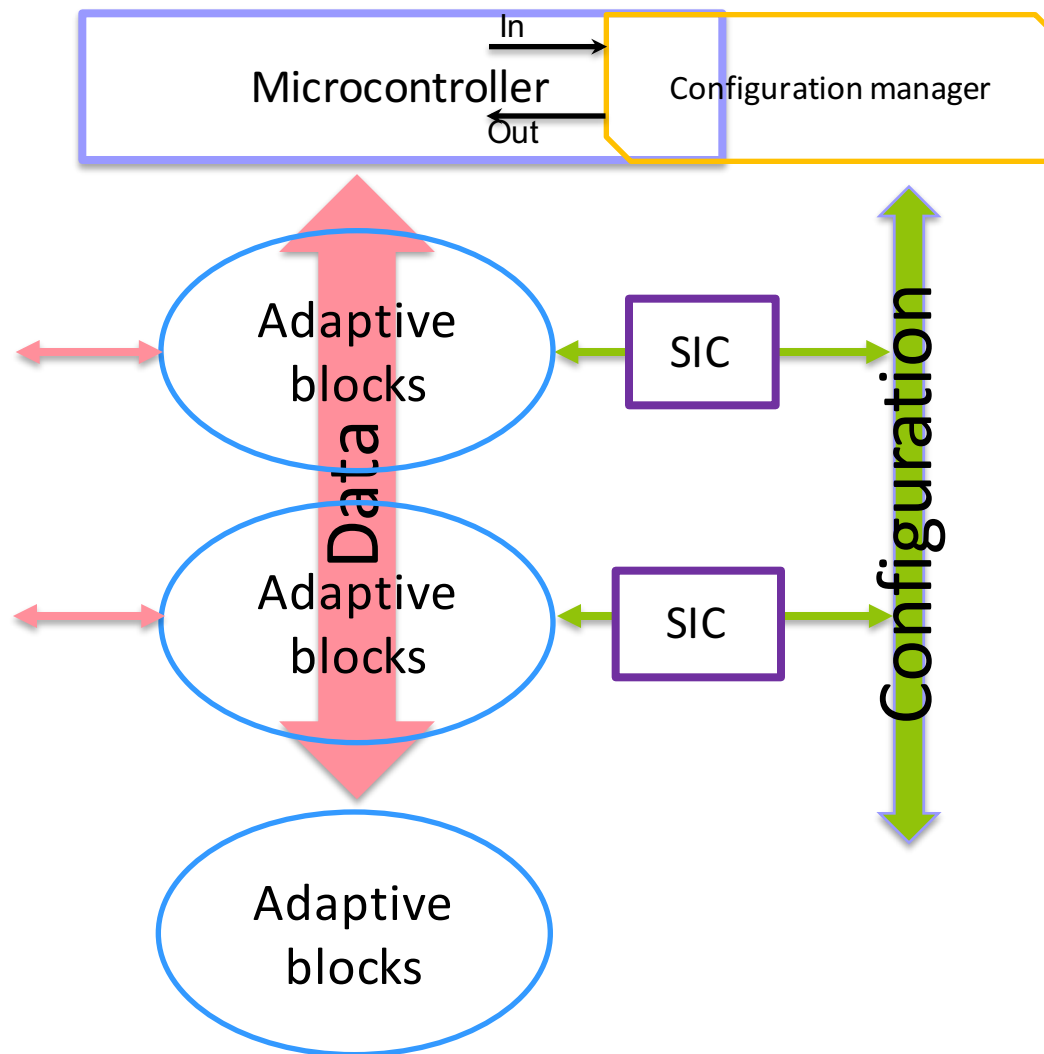
■ CHAIN

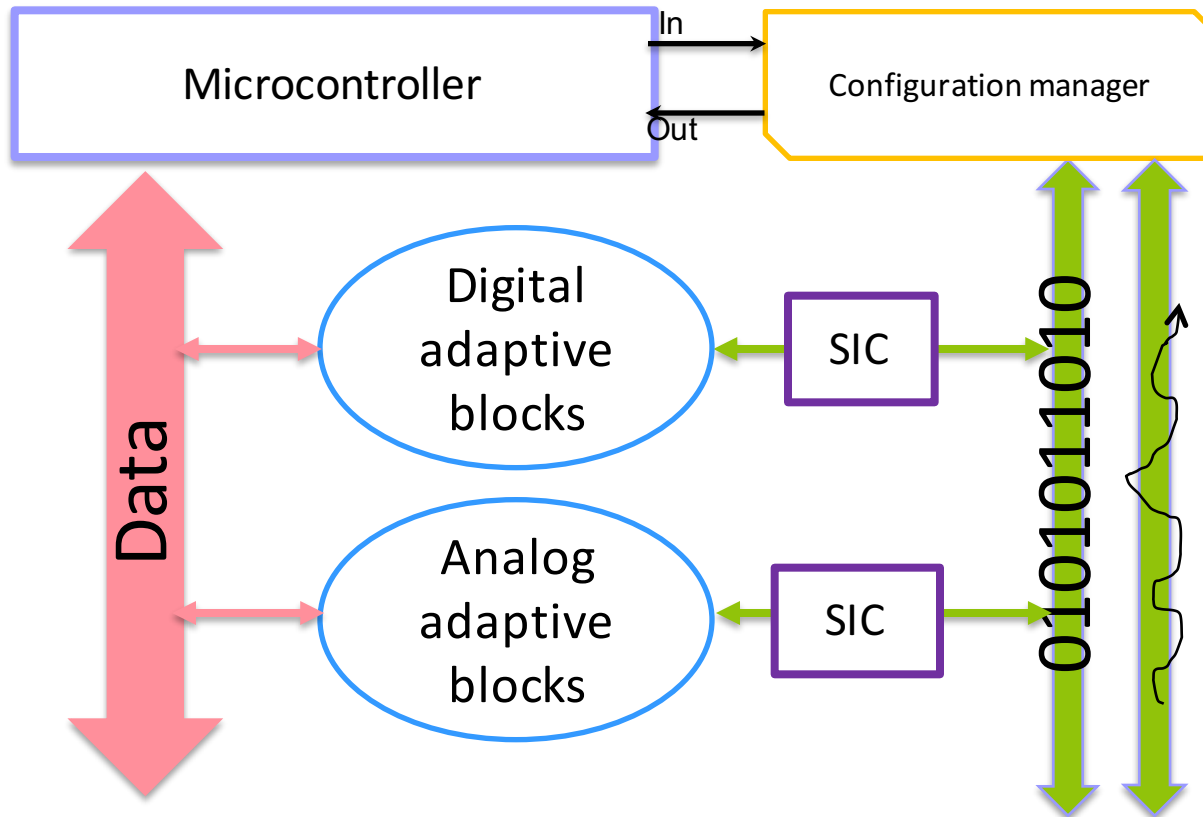
- Delay
- Use of
- High s



[3] <http://apt.cs.manchester.ac.uk/projects/interconnect/>

Problem: these networks are used for servicing multi-core chips, to bypass latency problems, or to target specific applications [2]Madduri,S. DATE 2009



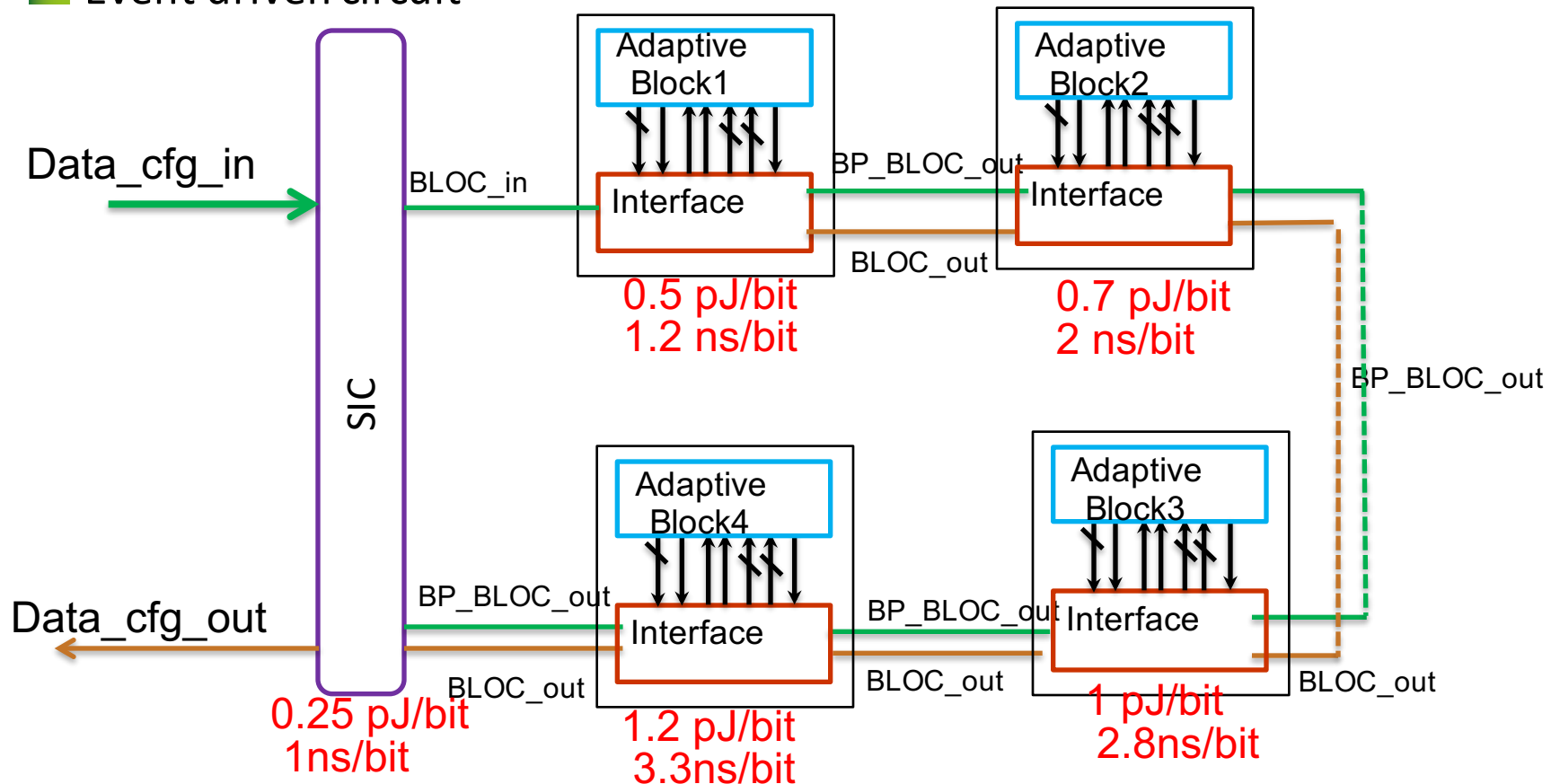


First implem: digital configuration

■ Asynchronous QDI logic ■ Network

- Robustness
- Quick wake up
- Event driven circuit

- Serial Interface Controller
- Interface



■ Conclusion

- Reconfiguration network for adaptive blocks in a WSN node circuit
 - **Not only for digital blocks (usual) but also for analog blocks**
- Asynchronous logic implementation
- Low cost and low energy network
- Reconfiguration of Frequency Locked Loop as example

■ Perspectives

- Digital configuration hardware implementation and fabrication
- Analog Block reconfiguration mechanisms



Thank you

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