CURRICULUM VITAE (Abridged Version)

July, 2006

1 PERSONAL DATA

Name: Ney Laert Vilar Calazans
Date of Birth: 15/10/1959, Maceió/AL - Brazil
Passport No.: CP 556393

2 ACADEMIC BACKGROUND/TITLES

1989 - 1993 Ph.D. in Applied Sciences, Group Electricity.
Université Catholique de Louvain, U.C.L., Belgium.
Thesis Title: State Minimization and State Assignment of Finite State Machines: their relationship and their impact on the implementation. Obtained in: 1993.
Thesis Advisor: Marc Davio (in memoriam) and Anne Marie Anckaert Trullemans.
Scholarship from: CNPq, Brazil.

1985 - 1988 Masters in Computer Science.
Universidade Federal do Rio Grande do Sul, UFRGS, Rio Grande do Sul, Brazil.
Dissertation Title: CIPREDI: Initial Contribution to a Method for the Design of Pre-Diffused Integrated Circuits. Obtained in: 1988.
Dissertation Advisor: Dante Augusto Couto Barone.
Scholarship from: CNPQ, Brazil.

1978 - 1985 Undergraduate Course in Electrical Engineering.
Universidade Federal do Rio Grande do Sul, UFRGS, Rio Grande do Sul, Brazil.

3 PROFESSIONAL ACTIVITIES

Pontifícia Universidade Católica do Rio Grande do Sul - PUCRS

Institutional Positions

1999 - Now Professor.
1994 - 1998 CNPq Scholarship from productivity in Research, Level: II-C.
1993 - 1999 Associate Professor.
1986 - 1993 Assistant Professor.

Activities

3/1986 - Now Teaching at Undergraduate and Graduate Levels

Undergraduate Courses (Computer Science and Computer engineering Courses)

1. Digital Circuits.
2. Computer Organization.
3. Computer Organization Laboratory.
4. Computer Architecture.
5. Special Topics in Digital Systems I.
6. Special Topics in Digital Systems II.
7. Microprogramming.

Graduate Courses (M.Sc. and Ph.D. in Computer Science)

1. Automated Synthesis and Prototyping of VLSI Systems.
2. Rapid Prototyping and Reconfigurable Computing.
3. VLSI Systems Design.
4. VLSI Design.
1. Parallel Architectures and Systems.
5. Distributed and Parallel Programming.
6. Algorithm Complexity and Optimization.
7. CAD Tools for VLSI.
8. Logic and Computing Theory.
9. Computing Systems II.
10. Theoretical Computing.
11. Engineering Systems.
12. Digital Systems and Computer Architecture.

3/2001 - 2/2002 Administrative activities at the Graduate (PPGCC) and Undergraduate Programs in Computer Science and Computer Engineering.

Positions

1. PPGCC Coordinator (in 1996-1997)
2. Member of the Coordinating Committee of the PPGCC. (in 1994-1995, 2001, 2004-now)
3. Member of the Coordinating Committee of the B.Sc. Course in Computer Science (in 2004-2005).
4. Member of the Coordinating Committee of the B.Sc. Course in Computer Engineering (in 2002-now)

Universidade Federal do Rio Grande do Sul - UFRGS

Institutional Positions
1988 - 1989 Research Engineer
1985 - 1988 Research Assistant
1980 - 1984 Undergraduate Research Student with CNPq Scholarship

Digitel S A Electronics Industry - DIGITEL

Institutional Position
1984 - 1985 Development Engineer.

Activities
4/1984 - 9/1985 Videotext Design Group.

4 PRIZES

2005 Best Conceptual Design in the DATE´2005 Designers Forum, European Community Europractice.
2005 II Xilinx Student Contest - First Place, Xilinx Inc.
2004 I Xilinx Student Contest - First Place, Xilinx Inc.
2002 Outstanding paper in its subject area in the SBCCI 2002, SBC - SBMICRO.

5 SCIENTIFIC PRODUCTION

5.1 PUBLISHED BOOKS AND BOOK CHAPTERS

1. MORAES, Fernando Gehm; CALAZANS, Ney Laert Vilar; MÖLLER, Leandro Heleno; BRIÃO, Eduardo Wenzel, CARVALHO, Ewerson Luiz de Souza. Dynamic and Partial Reconfiguration in FPGA SoCs: Requirements and Tools. Chapter 13. In: New Algorithms, Architectures and Applications for Reconfigurable Computing, edited by Patrick LYSAGHT & Wolfgang ROSENSTIEL. Springer. 2005. 313 pages.

2. CALAZANS, Ney Laert Vilar. Automated Design of Sequential Digital Systems. Rio de Janeiro: Imprinta Gráfica e Editora Ltda - UFRJ. 342 pages. 1998. (Book published in the context of the 11th. Computing School, realized from 20-24 July 1998)(In Portuguese)

5.2 ARTICLES PUBLISHED IN JOURNALS

1. MARCON, César Augusto Missio; PALMA, José Carlos Sant'anna; CALAZANS, Ney Laert Vilar; MORAES, Fernando Gehm. Design and Prototyping of an SDH-E1 Mapper Soft-core. Journal of the Brazilian Telecommunications Society, Campinas, vol 20, n. 2, p. 74-82, August, 2005.

2. MORAES, Fernando Gehm; CALAZANS, Ney Laert Vilar; MELLO, Aline Vieira de; MÖLLER, Leandro Heleno; OST, Luciano Copello. HERMES: an Infrastructure for Low Area Overhead Packet-switching Networks on Chip. Integration The VLSI Journal, Amsterdam, v. 38, n. 1, p. 69-93, October, 2004.

3. PALMA, José Carlos Sant'anna; MELLO, Aline Vieira de; MÖLLER, Leandro Heleno; MORAES, Fernando Gehm; CALAZANS, Ney Laert Vilar. Core Communication Interface for FPGAs. Journal Of Integrated Circuits And Systems, Porto Alegre, v. 1, n. 1, p. 44-51, March 2004.

4. MORAES, Fernando Gehm; CALAZANS, Ney Laert Vilar; MARCON, César Augusto Missio; MESQUITA, Daniel; PALMA, José Carlos Sant'anna; BLAUTH, Victor Hugo. Design and Prototyping of an E1 Drop_Insert Soft Cores. IEE Proceedings - Communications, London, v. 150, n. 4, pp. 239-243, August, 2003.

5. CALAZANS, Ney Laert Vilar; MORAES, Fernando Gehm. Integrating the Teaching of Computer Organization and Architecture with Digital Hardware Design Early in Undergraduate Courses. IEEE Transactions on Education, Piscataway, v. 44, n. 2, pp. 109-119, 2001. May, 2001.

6. CALAZANS, Ney Laert Vilar; MORAES, Fernando Gehm; TOROK, Delfim Luiz; ANDREOLI, Andrey Vedana. Design for Prototyping of a MAC Ethernet IP soft Core. Journal of Theoretical and Applied Informatics (RITA), Porto Alegre, v. 8, n. 1, pp. 23-41, 2001. (in Portuguese)

5.3 ARTICLES PUBLISHED IN CONFERENCE PROCEEDINGS

1. TEDESCO, Leonel Pablo; MELLO, Aline Vieira de; GIACOMET, Leonardo Luigi; CALAZANS, Ney Laert Vilar; MORAES, Fernando Gehm. Application Driven Traffic Modeling for NoCs. In: 19TH SYMPOSIUM ON INTEGRATED CIRCUITS AND SYSTEMS DESIGN - SBCCI 2006, Ouro Preto. 19th SBCCI. New York: ACM, 2006. Approved for publication.

2. MÖLLER, Leandro Heleno; SOARES, Rafael Iankowski; CARVALHO, Ewerson Luiz de Souza; GREHS, Ismael; CALAZANS, Ney Laert Vilar; MORAES, Fernando Gehm. Infrastructure for Dynamic Reconfigurable Systems:

Choices and Trade-offs. In: 19TH SYMPOSIUM ON INTEGRATED CIRCUITS AND SYSTEMS DESIGN - SBCCI 2006, Ouro Preto. 19th SBCCI. 2006. Approved for publication.

3. MÖLLER, Leandro Heleno; GREHS, Ismael; CALAZANS, Ney Laert Vilar; MORAES, Fernando Gehm. Reconfigurable Systems Enabled by a Network-on-Chip. In: 16TH INTERNATIONAL CONFERENCE ON FIELD PROGRAMMABLE LOGIC AND APPLICATIONS, 2006, Madrid. FPL 2006. 2006. Approved for publication.

4. MARCON, César Augusto Missio; PALMA, José Carlos Sant´anna; CALAZANS, Ney Laert Vilar; SUSIN, Altamiro Amadeu; REIS, Ricardo Augusto da Luz; MORAES, Fernando Gehm. Modeling the Traffic Effect for the Application Cores Mapping Problem onto NoCs. In: IFIP INTERNATIONAL CONFERENCE ON VERY LARGE SCALE INTEGRATION, 2005, Perth. IFIP VLSI-SOC 2005. 2005.

5. MELLO, Aline Vieira de; TEDESCO, Leonel Pablo; CALAZANS, Ney Laert Vilar; MORAES, Fernando Gehm. Virtual Channels in Networks on Chip: Implementation and Evaluation on Hermes NoC. In: 18TH SYMPOSIUM ON INTEGRATED CIRCUITS AND SYSTEMS DESIGN - SBCCI 2005. New York: ACM Press, 2005. pp. 178-183.

6. TEDESCO, Leonel Pablo; MELLO, Aline Vieira de; CALAZANS, Ney Laert Vilar; MORAES, Fernando Gehm. Traffic Generation and Performance Evaluation for Mesh-based NoCs. In: 18TH SYMPOSIUM ON INTEGRATED CIRCUITS AND SYSTEMS DESIGN - SBCCI 2005. New York: ACM Press, 2005. pp. 184-189.

7. PALMA, José Carlos Sant'anna; MARCON, César Augusto Missio; MORAES, Fernando Gehm; CALAZANS, Ney Laert Vilar; REIS, Ricardo Augusto da Luz; SUSIN, Altamiro Amadeu. Mapping Embedded Systems onto NoCs - The Traffic Effect on Dynamic Energy Estimation. In: 18TH SYMPOSIUM ON INTEGRATED CIRCUITS AND SYSTEMS DESIGN - SBCCI 2005. New York: ACM Press, 2005. pp. 196-201.

8. MARCON, César Augusto Missio; KREUTZ, Márcio; SUSIN, Altamiro Amadeu; CALAZANS, Ney Laert Vilar. Models for Embedded Application Mapping onto NoCs: Timing Analysis. In: 16TH IEEE INTERNATIONAL WORKSHOP ON RAPID SYSTEM PROTOTYPING, 2005 - RSP 2005, Montreal. 2005. pp. 17-23.

9. MARCON, César Augusto Missio; CALAZANS, Ney Laert Vilar; MORAES, Fernando Gehm; SUSIN, Altamiro Amadeu; REIS, Igor Maicá; HESSEL, Fabiano Passuelo. Exploring NoC Mapping Strategies: An Energy and Timing Aware Technique. In: DESIGN, AUTOMATION AND TEST IN EUROPE CONFERENCE AND EXHIBITION - DATE´05, Munich. 2005. pp. 502-507, Volume 1.

10. KREUTZ, Márcio; MARCON, César Augusto Missio; CALAZANS, Ney Laert Vilar; SUSIN, Altamiro Amadeu. Energy and Latency Evaluation of NoC Topologies. In: 2005 IEEE SYMPOSIUM ON CIRCUITS AND SYSTEMS, 2005, Kobe. ISCAS 2005. 2005. p. 5866-5869.

11. MELLO, Aline Vieira de; MÖLLER, Leandro Heleno; CALAZANS, Ney Laert Vilar; MORAES, Fernando Gehm. MultiNoC: A Multiprocessing System Enabled by a Network on Chip. In: DESIGN, AUTOMATION AND TEST IN EUROPE CONFERENCE AND EXHIBITION - DATE´05, 2005, Munich. DATE 2005 Designers' Forum Proceedings, Munich. 2005. pp. 234-239.

12. OST, Luciano Copello; MELLO, Aline Vieira de; PALMA, José Carlos Sant´anna; MORAES, Fernando Gehm; CALAZANS, Ney Laert Vilar. MAIA - A Framework for Networks on Chip Generation and Verification. In: ASIA SOUTH PACIFIC DESIGN AUTOMATION CONFERENCE, 2005, Beijing. ASP-DAC 2005. 2005. v. 1, p. 49-52.

13. CALAZANS, Ney Laert Vilar; MORAES, Fernando Gehm; MARCON, César Augusto Missio; PALMA, José Carlos Sant´anna. Design, Validation and Prototyping of the EMS SDH STM-1 Mapper Soft-core. In: 6TH IEEE LATIN-AMERICAN TEST WORKSHOP, 2005, Salvador. LATW 2005. 2005. p. 313-318.

14. MÖLLER, Leandro Heleno; MORAES, Fernando Gehm; CALAZANS, Ney Laert Vilar. Reconfigurable Processors: State of the Art. In: XI WORKSHOP IBERCHIP, 2005, Salvador. 2005. p. 110-113. (In Portuguese)

15. CARUSO, Luís Carlos Mieres; GUINDANI, Guilherme Montez; SCHMITT, Hugo Artur Weber; CALAZANS, Ney Laert Vilar; MORAES, Fernando Gehm. Sea of Processors Architecture for Network Intrusion Detection. In: XI WORKSHOP IBERCHIP, 2005, Salvador. 2005. v. 1, p. 247-250. (In Portuguese)

16. CARARA, Everton Alceu; MELLO, Aline Vieira de; CALAZANS, Ney Laert Vilar; MORAES, Fernando Gehm. Virtual Channels in Intra-chip Networks - Implementation in the Hermes Network. In: XI WORKSHOP IBERCHIP, 2005, Salvador. 2005. v. 1, p. 320-321. (In Portuguese)

17. CARVALHO, Ewerson Luiz de Souza; CALAZANS, Ney Laert Vilar; MORAES, Fernando Gehm; MESQUITA, Daniel. Reconfiguration Control for Dynamically Reconfigurable Systems. In: XIX CONFERENCE ON DESIGN OF CIRCUITS AND INTEGRATED SYSTEMS, 2004, Bordeaux. DCIS´2004. 2004. p. 405-410.

18. CARVALHO, Ewerson Luiz de Souza; CALAZANS, Ney Laert Vilar; BRIÃO, Eduardo Wenzel; MORAES, Fernando Gehm. PADReH - A Framework for the Design and Implementation of Dynamically and Partially Reconfigurable Systems. In: 17TH SYMPOSIUM ON INTEGRATED CIRCUITS AND SYSTEMS DESIGN - SBCCI 2004, 2004, Ipojuca. 17th Symposium on Integrated Circuits and Systems Design - SBCCI 2004. New York: ACM Press, 2004. pp. 10-15.

19. MÖLLER, Leandro Heleno; CALAZANS, Ney Laert Vilar; MORAES, Fernando Gehm; BRIÃO, Eduardo Wenzel; CARVALHO, Ewerson Luiz de Souza; CAMOZZATO, Daniel. FiPRe: An Implementation Model to Enable Self-Reconfigurable Applications. In: FPL - THE INTERNATIONAL CONFERENCE ON FIELD PROGRAMMABLE LOGIC AND APPLICATIONS, 2004, Antwerp, Belgium. FPL'04. Berlin: Springer-Verlag, 2004. pp. 1042-1046.

20. MARCON, César Augusto Missio; AMORY, Alexandre Morais; LUBASZEWSKI, Marcelo Soares; SUSIN, Altamiro Amadeu; CALAZANS, Ney Laert Vilar; MORAES, Fernando Gehm; HESSEL, Fabiano Passuelo. Applying Memory Test to Embedded Systems. In: 5TH IEEE LATIN-AMERICAN TEST WORKSHOP, 2004, Cartagena. LATW 2004. 2004.

21. CARVALHO, Ewerson Luiz de Souza; MÖLLER, Frederico Bartz; MORAES, Fernando Gehm; CALAZANS, Ney Laert Vilar. Configuration Control in Dynamically and Partially Reconfigurable Systems. In: X WORKSHOP IBERCHIP, 2004, Cartagena. X Workshop Iberchip. 2004. (In Portuguese)

22. MORENO, Edson Ifarraguirre; RODOLFO, Taciano Ares; CALAZANS, Ney Laert Vilar. SoC Modeling and Description at Different Abstraction Levels. In: X WORKSHOP IBERCHIP, 2004, Cartagena. X Workshop Iberchip. 2004. (In Portuguese)

23. MORAES, Fernando Gehm; OST, Luciano Copello; MELLO, Aline Vieira de; PALMA, José Carlos Sant'anna; CALAZANS, Ney Laert Vilar. NOCGEN - A Tool for the Generation of Intra-chip Networks based on the HERMES Infra-structure. In: X WORKSHOP IBERCHIP, 2004, Cartagena. X Workshop Iberchip. 2004. (In Portuguese)

24. BRIÃO, Eduardo Wenzel; CAMOZZATO, Daniel; RIES, Luís Henrique Leal; MORAES, Fernando Gehm; CALAZANS, Ney Laert Vilar. Partial and Dynamic Reconfiguration of Intellectual Property Cores with Standardized Communication Interfaces. In: X WORKSHOP IBERCHIP, 2004, Cartagena. X Workshop Iberchip. 2004. (In Portuguese)

25. MORAES, Fernando Gehm; MELLO, Aline Vieira de; MÖLLER, Leandro Heleno; OST, Luciano Copello; CALAZANS, Ney Laert Vilar. A Low Area Overhead Packet-switched Network on Chip: Architecture and Prototyping. In: IFIP International Conference on Very Large Scale Integration, VLSI-SoC 2003. Darmstadt, Germany. pp. 318-323, 2003.

26. CALAZANS, Ney Laert Vilar; MORENO, Edson; HESSEL, Fabiano; ROSA, Vitor, MORAES, Fernando Gehm; CARARA, Everton. From VHDL Register Transfer Level to SystemC Transaction Level Modeling: a comparative case study. In: 16TH SYMPOSIUM ON INTEGRATED CIRCUITS AND SYSTEMS DESIGN, SBCCI´2003. Los Alamitos: IEEE Computer Society Press. São Paulo, Brazil. pp. 355-360, 2003.

27. MESQUITA, Daniel; MORAES, Fernando Gehm; PALMA, José Carlos Sant'anna; MÖLLER, Leandro Heleno; CALAZANS, Ney Laert Vilar. Development of a Tool-Set for Remote and Partial Reconfiguration of FPGAs. In: Design, Automation and Test in Europe Conference and Exhibition, DATE´03. Munich, Germany. pp. 1122-1123. 2003.

28. MESQUITA, Daniel; MORAES, Fernando Gehm; PALMA, José Carlos Sant'anna; MÖLLER, Leandro Heleno; CALAZANS, Ney Laert Vilar. Remote and Partial Reconfiguration of FPGAs: tools and trends. In: 10TH RECONFIGURABLE ARCHITECTURES WORKSHOP, RAW´03. Nice, France. 2003.

29. MARCON, César Augusto Missio; HESSEL, Fabiano Passuelo; AMORY, Alexandre Morais; RIES, Luís Henrique Leal; MORAES, Fernando Gehm; CALAZANS, Ney Laert Vilar. Prototyping of Embedded Digital Systems from SDL Language: a case study. In: SEVENTH ANNUAL IEEE INTERNATIONAL WORKSHOP ON HIGH LEVEL DESIGN VALIDATION AND TEST, HLDVT´02. Cannes, France. pp. 133-138. 2002.

30. BEZERRA, Eduardo Augusto; POUCHET, Marianne; CALAZANS, Ney Laert Vilar; MORAES, Fernando Gehm; GOUGH, Michael. An Adaptable Educational Platform for Engineering and IT Laboratory Based Courses. In: 2002 FRONTIERS IN EDUCATION CONFERENCE, FIE´02. Boston, MA. 2002.

31. CALAZANS, Ney Laert Vilar; MORAES, Fernando Gehm; MARCON, César Augusto Missio. Teaching Computer Organization and Architecture with Hands-on Experience. In: 2002 FRONTIERS IN EDUCATION CONFERENCE, FIE´02. Boston, MA. 2002.

32. PALMA, José Carlos Sant'anna; MELLO, Aline Vieira de; MORAES, Fernando Gehm; CALAZANS, Ney Laert Vilar. Core Communication Interface for FPGAs. In: 15TH SYMPOSIUM ON INTEGRATED CIRCUITS AND SYSTEMS DESIGN, SBCCI´2002. Los Alamitos: IEEE Computer Society Press. Porto Alegre, Brazil. 2002.

33. AMORY, Alexandre Morais; MORAES, Fernando Gehm; OLIVEIRA, Leandro Augusto de; CALAZANS, Ney Laert Vilar; HESSEL, Fabiano Passuelo. A Heterogeneous and Distributed Co-Simulation Environment. In: 15TH SYMPOSIUM ON INTEGRATED CIRCUITS AND SYSTEMS DESIGN, SBCCI´2002. Los Alamitos: IEEE Computer Society Press. Porto Alegre, Brazil. 2002.

34. MARCON, César Augusto Missio; CALAZANS, Ney Laert Vilar; MORAES, Fernando Gehm. Requirements, Primitives and Models for Systems Specification. In: 15TH SYMPOSIUM ON INTEGRATED CIRCUITS AND SYSTEMS DESIGN, SBCCI´2002. Los Alamitos: IEEE Computer Society Press. Porto Alegre, Brazil. 2002.

35. MORAES, Fernando Gehm; ZORZO, Avelino Francisco; CALAZANS, Ney Laert Vilar. Deriving Different Computer Science Curricula from a Common Core of Disciplines. In: INFORMATICS CURRICULA, TEACHING METHODS AND BEST PRACTICE, ICTEM'2002. Florianópolis, Brazil. pp. 43-49. 2002.

36. AMORY, Alexandre Morais; MORAES, Fernando Gehm; OLIVEIRA, Leandro Augusto de; HESSEL, Fabiano Passuelo; CALAZANS, Ney Laert Vilar. Development of a Distributed and Heterogeneous Cossimulation Environment. In: VIII WORKSHOP IBERCHIP. Guadalajara, Mexico. 2002. (in Portuguese)

37. PALMA, José Carlos Sant'anna; MELLO, Aline Vieira de; CALAZANS, Ney Laert Vilar; MORAES, Fernando Gehm. Core Communication Interface in FPGAs. In: VIII WORKSHOP IBERCHIP. Guadalajara, Mexico. 2002. (in Portuguese)

38. MARCON, César Augusto Missio; CALAZANS, Ney Laert Vilar; MORAES, Fernando Gehm; RIES, Luís Henrique Leal; HESSEL, Fabiano Passuelo. Modeling and Description of Computing Systems: a case study comparing VHDL and SDL languages. In: VIII WORKSHOP IBERCHIP. Guadalajara, Mexico. 2002. (in Portuguese)

39. MORAES, Fernando Gehm; AMORY, Alexandre Morais; CALAZANS, Ney Laert Vilar; BEZERRA, Eduardo Augusto; PETRINI JÚNIOR, Juracy. Using the CAN Protocol and Reconfigurable Computing Technology For Web-Based Smart House Automation. In: 14TH SYMPOSIUM ON INTEGRATED CIRCUITS AND SYSTEMS DESIGN - SBCCI´2001. Los Alamitos: IEEE Computer Society Press. Pirenópolis, Brazil. 2001.

40. CALAZANS, Ney Laert Vilar; MORAES, Fernando Gehm; MARCON, César Augusto Missio; BLAUTH, Vitor Hugo; VALIATI, Ronaldo; MANFROI, Édison. Effective Industry-Academia Cooperation in Telecom: a method, a case study and some initial results. In: XIX SIMPÓSIO BRAZILEIRO DE TELECOMUNICAÇÕES, SBrT´2001. Fortaleza, Brazil. 2001.

41. CAPPELATTI, Ewerton Artur; MORAES, Fernando Gehm; CALAZANS, Ney Laert Vilar; OLIVEIRA, Leandro Augusto de. High Performance Bus for Hardware/Software Interaction. In: VII WORKSHOP IBERCHIP IWS'2001, IWS'2001. Montevideo, Uruguay. 2001. (in Portuguese)

42. TOROK, Delfim Luiz; CALAZANS, Ney Laert Vilar; MORAES, Fernando Gehm; ANDREOLI, Andrey Vedana. Design, Implementation and Validation of an Ethernet IP Soft Core on reconfigurable Devices. In: VII WORKSHOP IBERCHIP, WS'2001, IWS'2001. Montevideo, Uruguay. 2001 (in Portuguese)

43. MESQUITA, Daniel; MORAES, Fernando Gehm; PALMA, José Carlos Sant'anna; MÖLLER, Leandro; CALAZANS, Ney Laert Vilar. Partial and Remote Core Reconfiguration in FPGAs. In: VII WORKSHOP IBERCHIP, IWS'2001. Montevideo, Uruguay. 2001. (in Portuguese)

44. MORAES, Fernando Gehm; CALAZANS, Ney Laert Vilar; MARCON, César Augusto Missio; MELLO, Aline Vieira de. A Compiling and Simulation Environment for Parameterizable Embedded Processors. In: VII WORKSHOP IBERCHIP, IWS'2001. Montevideo, Uruguay. 2001. (in Portuguese)

45. MORAES, Fernando Gehm; MELLO, Aline Vieira de; CALAZANS, Ney Laert Vilar. Embedded Processor Development Environment for Codesign Applications. In: SEMINÁRIO DE COMPUTAÇÃO RECONFIGURÁVEL, SCR'2001.Belo Horizonte, Brazil. 2001. (in Portuguese)

46. PALMA, José Carlos Sant'anna; MORAES, Fernando Gehm; CALAZANS, Ney Laert Vilar. Methods for Development and Distribution of IP Cores. In: SEMINÁRIO DE COMPUTAÇÃO RECONFIGURÁVEL, SCR'2001.Belo Horizonte, Brazil. 2001. (in Portuguese)

47. BEZERRA, Eduardo Augusto; POUCHET, Marianne; STIPIDIS, Elias; MORAES, Fernando Gehm; CALAZANS, Ney Laert Vilar; EINSFELDT, Augusto. RECKON - A reconfigurable prototyping kit for engineering and IT laboratory based courses. In: SEMINÁRIO DE COMPUTAÇÃO RECONFIGURÁVEL, SCR'2001.Belo Horizonte, Brazil. 2001.

48. MESQUITA, Daniel; MORAES, Fernando Gehm; MÖLLER, Leandro; CALAZANS, Ney Laert Vilar. Remote and Partial Reconfiguration of Virtex Family FPGA Devices. In: SEMINÁRIO DE COMPUTAÇÃO RECONFIGURÁVEL, SCR'2001.Belo Horizonte, Brazil. 2001. (in Portuguese)

49. CALAZANS, Ney Laert Vilar; MORAES, Fernando Gehm; QUINTANS, Katherine Beserra; NEUWALD, Felipe Barp. Accelerating Sorting through the Use of Reconfigurable Hardware. In: Reconfigurable Computing - Experiences and Perspectives. Marília, Brazil. pp. 30-35. 2000.

50. MORAES, Fernando Gehm; CALAZANS, Ney Laert Vilar; FERREIRA, Ewerton Hofler; LIEDKE, Daniel Carvalho. Efficient Implementation of a Load/store Architecture in VHDL. In: Reconfigurable Computing - Experiences and Perspectives. Marília, Brazil. pp. 2-13. 2000. (in Portuguese)

51. CALAZANS, Ney Laert Vilar, MORAES, Fernando Gehm. VLSI Hardware Design by Computer Science Students: How early can they start? How far can they go?. In: 1999 FRONTIERS IN EDUCATION CONFERENCE, San Juan. IEEE Computer Society Press. pp.13612-13617. 1999.

52. MORAES, Fernando Gehm, CALAZANS, Ney Laert Vilar, SILVA, Felipe Rocha, BARRIOS, Maurício. Cleo-LIRMM: An Experiment of Dedicated Processors Implementation on Embedded Systems Prototyping Platforms. In: V WORKSHOP IBERCHIP, Lima, Peru. pp.81-90.1999. (in Portuguese)

53. MARQUES, Paulo César, MORAES, Fernando Gehm, CALAZANS, Ney Laert Vilar. PMAZE: Modeling and Routing for FPGAs. In: V WORKSHOP IBERCHIP, Lima, Peru. pp.70-80.1999. (in Portuguese)

54. CALAZANS, Ney Laert Vilar, MADEIRA, André Duque. ASSTUCE - An Exploratory Environment for Finite State Machines. In: XXIII CONFERENCIA LATINOAMERICANA DE INFORMÁTICA, CLEI, Valparaiso, Chile. v.1. pp.117-126.1997.

55. VARGAS, Fabian, MORAES, Fernando Gehm, CALAZANS, Ney Laert Vilar, BEZERRA, Eduardo Augusto. HardSoft: Reconfigurable Platform for Characterization under Radiation of Electronic Components Employed in Satellites. In: VII SIMPÓSIO DE COMPUTADORES TOLERANTES A FALHAS, SCTF. Campina Grande, Brazil. pp.139-152.1997. (in Portuguese)

56. CARNEIRO, Mára Lúcia Fernandes, CALAZANS, Ney Laert Vilar. Automated Design of Distillation Columns based on Probabilistic Optimization. In: XI CONGRESSO BRAZILEIRO DE ENGENHARIA QUÍMICA, COBEQ. Rio de Janeiro, Brazil. 1996. (in Portuguese)

57. VARGAS, Fabian, VELAZCO, Raoul, AMARAL, José Nelson, CALAZANS, Ney Laert Vilar, RODRIGUES, Alderico. Radiation effects on electronics: the need for ground tests. In: IX SIMPÓSIO BRAZILEIRO DE CONCEPÇÃO DE CIRCUITOS INTEGRADOS - SBCCI´96. Recife. Brazil. pp.105-116. 1996.

58. CALAZANS, Ney Laert Vilar. Considering State Minimization during State Assignment. In: I IBERO AMERICAN MICROELECTRONICS CONFERENCE - X CONGRESS OF THE BRAZILIAN MICROELECTRONICS SOCIETY, Canela, RS. pp.49-58. 1995.

59. CALAZANS, Ney Laert Vilar. Boolean Constrained Encoding: a new formulation and a case study. In: INTERNATIONAL CONFERENCE ON COMPUTER-AIDED DESIGN - ICCAD´94, San Jose, CA. pp.702-706. 1994.

60. CALAZANS, Ney Laert Vilar, ZHANG, Qinhai, JACOBI, Ricardo Pezzuol, YERNAUX, Bruno, TRULLEMANS, Anne Marie. Advanced Ordering and Manipulation Techniques for Binary Decision Diagrams. In: EUROPEAN CONFERENCE ON DESIGN AUTOMATION, EDAC'92. Brussels, Belgium. pp.452-457. 1992.

61. CALAZANS, Ney Laert Vilar. State Minimization and State Assignment of Finite State Machines. their relationship and their impact on the implementation. In: IFIP INTERNATIONAL WORKSHOP ON APPLICATION-ORIENTED SYNTHESIS. Dresden, Germany. 1992.

62. CALAZANS, Ney Laert Vilar, JACOBI, Ricardo Pezzuol, ZHANG, Qinhai, TRULLEMANS, Charles. Improving BDDs manipulation through incremental reduction and enhanced heuristics. In: CUSTOM INTEGRATED CIRCUITS CONFERENCE, CICC´91. San Diego, CA. pp.1131-1135. 1991. (Presentation Slides)

63. JACOBI, Ricardo Pezzuol, CALAZANS, Ney Laert Vilar, TRULLEMANS, Charles. Incremental Reduction of Binary Decision Diagrams. In: INTERNATIONAL SYMPOSIUM ON CIRCUITS AND SYSTEMS, ISCAS'91. Singapore, Singapore. pp.3174-3177. 1991.

64. CALAZANS, Ney Laert Vilar, WEBER, Taisy da Silva. Logic Minimization for Combinational Circuits. In: IV SIMPÓSIO BRAZILEIRO DE CONCEPÇÃO DE CIRCUITOS INTEGRADOS, SBCCI. Rio de Janeiro, Brazil. pp.52-61. 1989. (in Portuguese)

65. CALAZANS, Ney Laert Vilar, REY, Leandro Fortes, WAGNER, Flávio Rech. A Logic Simulator for an Integrated Environment of Digital Hardware Design. In: III CONGRESSO DA SOCIEDADE BRAZILEIRA DE MICROELETRÔNICA, SBMICRO. São Paulo, Brazil. pp.385-395. 1988.

66. CALAZANS, Ney Laert Vilar. Specification of EDGAR - A Mask Editor for Gate Array Integrated Circuits. In: XIV SEMINÁRIO INTEGRADO DE SOFTWARE E HARDWARE, SEMISH. Salvador, Brazil. pp.117-130. 1987. (in Portuguese)

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5.4 Advised or Presented Thesis and Dissertations

1. BASTOS, Érico Nunes Ferreira. Mercury: An intra-chip Network with 2D Torus Topology and Adaptive Routing. January 2006. 148 pages. Scholarship Sponsor: CAPES. (Presented and approved. Research Advisor: Ney Laert Vilar Calazans) (In Portuguese)

2. SOARES, Rafael Iankowski. Reconfigurable Hardware Configuration Control in Software: Infrastructure and Implementation. MSc Dissertation, PPGCC - FACIN - PUCRS, Porto Alegre, Brazil. January 2006. 145 pages. Scholarship Sponsor: CAPES. (Presented and approved. Research Advisor: Ney Laert Vilar Calazans) (In Portuguese).

3. MARCON, César Augusto Missio. Models for Applications Mapping in Intrachip Communication Infra-structures. PhD Thesis, PPGC - II - UFRGS, Porto Alegre, Brazil. December 2005. 192 pages. Scholarship Sponsor: CAPES. (Presented and approved. Research Advisor: Altamiro Amadeu Susin. Research Co-Advisor: Ney Laert Vilar Calazans) (In Portuguese)

4. MORENO, Edson Ifarraguirre. Modeling, Description and Validation of Intra-Chip Networks at the Transaction Level. MSc Dissertation, PPGCC - FACIN - PUCRS, Porto Alegre, Brazil. March 2004. 137 pages. Scholarship Sponsor: CAPES. (Presented and approved. Research Advisor: Ney Laert Vilar Calazans) (In Portuguese)

5. CARVALHO, Ewerson Luiz de Souza. RSCM - A Configuration Controller for Reconfigurable Hardware Systems. MSc Dissertation, PPGCC - FACIN - PUCRS, Porto Alegre, Brazil. March 2004. 155 pages. Scholarship Sponsor: CNPq. (Presented and approved. Research Advisor: Ney Laert Vilar Calazans) (In Portuguese)

6. BRIÃO, Eduardo Wenzel. Dynamic and Partial Reconfiguration for Intellectual Property Cores. MSc Dissertation, PPGCC - FACIN - PUCRS, Porto Alegre, Brazil. January 2004. 149 pages. Scholarship Sponsor: CNPq. (Presented and approved. Research Advisor: Ney Laert Vilar Calazans). (In Portuguese)

7. SOUZA, Sheila Moreira. ATM Adaptation Layers for the Transfer of Data and Voice. MSc Dissertation, PPGCC - FACIN - PUCRS, Porto Alegre, Brazil. January 2003. 151 pages. (Presented and approved. Research Advisor: Ney Laert Vilar Calazans) (In Portuguese)

8. CASTANHEIRA, Leonardo Dutra. Flexible Traffic Generation with Application to ATM Networks. MSc Dissertation, PPGCC - FACIN - PUCRS, Porto Alegre, Brazil. February 2003. 138 pages. (Presented and approved. Research Advisor: Ney Laert Vilar Calazans) (In Portuguese)

9. TOROK, Delfim Luiz. Design for Prototyping of the Medium Access Protocol in Ethernet Networks. MSc Dissertation, PPGCC - FACIN - PUCRS, Porto Alegre, Brazil. August 2001. 136 pages. (Presented and approved. Research Advisor: Ney Laert Vilar Calazans) (In Portuguese)

10. CARNEIRO, Mára Lúcia Fernandes. Automated Synthesis of Distillation Columns: an alternative approach to the design process. MSc Dissertation, PPGCC - FACIN - PUCRS, Porto Alegre, Brazil. September 1996. 107 pages. (Presented and approved. Research Advisor: Ney Laert Vilar Calazans) (In Portuguese)

11. CALAZANS, Ney Laert Vilar. State Minimization and State Assignment of Finite State Machines: their relationship and their impact on the implementation . PhD Thesis, Université Catholique de Louvain - UCL, Louvain-la-Neuve, Belgium. October 1993.

12. CALAZANS, Ney Laert Vilar. CIPREDI: Initial Contribution to a Design Method for Pre-Diffused Integrated Circuits. MSc Dissertation, Universidade Federal do Rio Grande do Sul - UFRGS, CPGCC, Porto Alegre, RS, Brazil. October, 1988. (in Portuguese)

6 COMPLEMENTARY DATA

6.1 ONGOING ADVISING

6.1.1 M. Sc. in Computer Science

1 PONTES, Julian José Hilgemberg. Non-synchronous Intra-chip Networks: implementation and prototyping. Start:2006. Pontifícia Universidade Católica do Rio Grande do Sul, CAPES Scholarship.

2 DISCONZI, Rosana Perazzolo. Behavioral Synthesis and Intra-chip Networks: from design capture to chip layout. Start:2005. Pontifícia Universidade Católica do Rio Grande do Sul.

3 SCHERER JUNIOR, Carlos Adail. Intra-chip Network Topologies: design exploration and performance evaluation. Start:2005. Pontifícia Universidade Católica do Rio Grande do Sul, CNPq Scholarship.

6.1.2 Ph.D. in Computer Science

1 SOARES, Rafael Iankowski. Abstract Modeling and Implementation of Intra-chip Communication Architectures. Start:2006. Pontifícia Universidade Católica do Rio Grande do Sul.

2 MORENO, Edson Ifarraguirre. Scheduling Applications onto Intra-chip Networks. Start:2005. Pontifícia Universidade Católica do Rio Grande do Sul, CNPq.

7 SCIENTIFIC PRODUCTION INDICATORS

Bibliographic Production

Published Complete Journal Articles - 7

Conference publications - 71
Complete - 64
Expanded Abstracts - 4

Books and Book Chapters - 2
Published Books - 1
Published Book Chapters - 1

Advising of Graduate Works (Concluded)

Masters – 9 as advisor

Ph.D. - 1 as Co-advisor

Complementary Data

Ongoing Student Advising - 5