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ASCEND-TSMC180-NCL: A SIMPLE NCL CELL LIBRARY TO SUPPORT MANUFACTURABLE QDI DESIGNS

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I dedicate this work to my family and to all my friends, specially to my grandparents without whom I could not achieve this.

“A man travels the world over in search of what he needs, and returns home to find it.”
(George Moore)

ASCEND-TSMC180-NCL: UMA BIBLIOTECA SIMPLES DE CÉLULAS NCL PARA SUPORTE AO PROJETO DE CIRCUITOS QDI FABRICÁVEIS

RESUMO

Circuitos digitais modernos podem conter bilhões de transistores, executando tarefas de computação extremamente complexas. O projeto baseado em células auxilia o processo de desenvolver circuitos integrados específicos para uma aplicação dada. Esta técnica exige uma biblioteca de células de suporte para intermediar a tradução de descrições alto nível de hardware, e.g. em Verilog ou VHDL, em um leiaute de circuito integrado fabricável. Existem numerosas bibliotecas disponíveis para elaborar circuitos síncronos. Infelizmente, poucas bibliotecas dão suporte ao projeto não-síncrono, e praticamente nenhuma destas está comercialmente disponível. Circuitos digitais assíncronos podem ser desenvolvidos usando diversos estilos lógicos. *Null Convention Logic* é um estilo entre os mais mencionados na literatura, conhecido por sua robustez a variações que perpassam o processo de projeto de circuitos integrados. Este trabalho propõe e descreve o desenvolvimento da ASCEnD-TSMC180-NCL, uma biblioteca de células que dá suporte à fabricação de circuitos digitais assíncronos. Catorze tipos de células com diferentes funções lógicas foram desenvolvidas, cada uma disponível em um conjunto de diferentes dimensionamentos. Até onde o Autor pode verificar, ASCEnD-TSMC180-NCL é poderosa o suficiente para permitir o projeto de circuitos usando um estilo de projeto derivado da *Null Convention Logic*. Como um projeto completo de um circuito integrado fabricável requer células especiais (e.g. pinos de E/S, espaçadores, uma variedade de *buffers* e inversores, células de antena, etc.), há vantagens em tornar uma biblioteca de células assíncronas compatível com uma biblioteca comercial escolhida, que forneça o conjunto complementar de células para habilitar projetos fabricáveis. Emprega-se aqui a biblioteca SAGE-X do ARM para tal compatibilidade. Um somador *pipeline* de 32 bits serviu para validar a biblioteca ASCEnD-TSMC180-NCL. Este circuito atesta a correção da implementação da biblioteca ASCEnD-TSMC180-NCL, integrando-a a um conjunto de ferramentas comerciais, o que forma um fluxo completo para o projeto de circuitos integrados digitais baseados nela.

Palavras-Chave: Circuitos assíncronos, Projeto baseado em células, Null convention logic, NCL, Quasi-delay insensitive, QDI, Biblioteca de células, leiaute de células.

ASCEND-TSMC180-NCL: A SIMPLE NCL CELL LIBRARY TO SUPPORT MANUFACTURABLE QDI DESIGNS

ABSTRACT

Modern digital circuits can encompass billions of transistors, and are able to execute immensely complex computation tasks. The design process of application specific integrated circuits this big benefits from using cell-based design techniques. Such techniques require the existence of a supporting library of component cells, which intermediates the translation of high level hardware descriptions in e.g. Verilog or VHDL into an integrated circuit manufacturable layout. There are currently numerous libraries available for the design of synchronous circuits. Unfortunately, few libraries support clockless design, and fewer, if any of these, are commercially available. Asynchronous digital circuits can be developed using one of several available logic templates. Null convention logic is one such template that is among the most mentioned in the literature, being known for its robustness to timing and other variations that plague the integrated circuit design process. This work proposes and describes the development of ASCEnD-TSMC180-NCL, a simple null convention logic cell library for supporting the manufacturing of asynchronous digital circuits. Fourteen cell types with different logic functions were developed, each available in a set of different drive strengths. As far as the Author could verify, ASCEnD-TSMC180-NCL is resourceful enough to allow the design of circuits using the spatially distributed dual-spacer null convention logic template, derived from the null convention logic template. However, since a complete integrated circuit design requires some special cells to be manufacturable (I/O cells, fillers, a large variety of buffers and inverters, antenna cells etc.), there are advantages in making an asynchronous cell library fully compatible with some selected commercial library, which can provide a complementary set of cells. In this work, the SAGE-X library from ARM was selected for compatibility. To validate the ASCEnD-TSMC180-NCL library, a pipelined adder circuit with eight 32-bit inputs was described and implemented. The design attests the correction of the ASCEnD-TSMC180-NCL library implementation, by integrating it with a set of commercial tools, thus forming a complete design flow for digital integrated circuits design based on this library.

Keywords: Asynchronous circuit, Cell-based design, Null convention logic, NCL, Quasi delay insensitive, QDI, Standard cell library, Cell layout.

LIST OF FIGURES

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LIST OF ACRONYMS

AMS – Analog Mixed-Signal

ARM – Advanced RISC Machine

BNF – Backus-Naur Form

CES – Cell Specifier

CMOS – Complementary Metal Oxide Semiconductor

DI – Delay Insensitive

DRC – Design Rule Checker

EDA – Electronic Design Automation

FPGA – Field-Programmable Gate Array

GAPH – Hardware Development Support Group

IC – Integrated Circuits

LEF – Library Exchange Format

LIB – Liberty

LVS – Layout vs Schematic

NCL – Null Convention Logic

NDA – Non-Disclosure Agreement

NMOS – N Metal Oxide Semiconductor

NRE – Non-Recurring Engineering

PEX – Parasitic Extraction

PMOS – P Metal Oxide Semiconductor

PVT – Process, Voltage and Temperature

QDI – Quasi Delay Insensitive

RISC – Reduced Instruction Set Computer

ROGEN – Ring Oscillator Generator

RTL – Register Transfer Level

SDDS-NCL – Spatially Distributed Dual-Spacer Null Convention Logic

SOC – System-on-Chip

SPICE – Simulation Program with Integrated Circuit Emphasis

TSMC – Taiwan Semiconductor Manufacturing Company

VF – Virtual Function

VHDL – VHSIC Hardware Description Language

VHSIC – Very-High-Speed Integrated Circuit

CONTENTS

1. INTRODUCTION AND MOTIVATION

In the past decades asynchronous digital circuit design has been a research subject for some research groups and companies. The design complexity of these do not currently allow them to be employed in large-scale projects. Meanwhile, the electronic design automation (EDA) industry developed a large number of tools and techniques intended to support almost exclusively synchronous designs. Nonetheless, as technology geometries get smaller, problems like power consumption density and clock skew inside chips started to become increasingly difficult to cope with.

Asynchronous design begins to re-emerge as a solution to the aforementioned issues. This approach has the ability to relieve designers from using a clock, substituting it by local handshake protocols, which potentially solve problems caused by synchronous design in newer technologies. Handhsake communication protocols are covered in some detail in Section 2.1.1. The discussion herein states the Author´s motivation to explore this area, brings the objectives of the work and reports its achieved contributions.

1.1 Motivation

One of the biggest problems with asynchronous design of digital circuits is where to learn about it. There are several books and articles discussing asynchronous advantages and inconveniences, but the subject is convoluted for several reasons, some of which are depicted next. First, most undergraduate courses, if not all, tend to focus on synchronous design only, and rarely explore alternatives to this well-established design approach. Second, asynchronous design is not a single discipline. There is a large number of design techniques outside the synchronous domain, and it is very hard to deal with the large diversity of alternative approaches. Third, electronic design automation (EDA) tools tend to strongly focus on supporting synchronous design alone, leaving asynchronous design techniques unattended by automated tools support.

As Moreira points out in [Mor16] about the design of integrated circuits (ICs): “Contemporary IC design styles trade off time to market, non-recurring engineering (NRE) costs, production cost per part and performance, area and energy efficiency. These design styles are often classified into full-custom and semi-custom approaches. In the former, all the aspects of an IC are handcrafted and the application is literally manually designed, from functional to physical level. This means that every transistor is individually sized and laid out, involving detailed manipulation of physical and electrical characteristics of these devices.” Examples of ICs designed using full-custom techniques are RAM and Flash memory

and microprocessor chips, since the sales scale of such circuits justify the huge design effort they require.

Designing using a full custom flow is very complex. As the project gets bigger, difficulties grow very fast. Full custom designs are highly optimized in terms of transistor positioning and in area utilization, compared to schemes where transistors are pre-fabricated, like in gate arrays or field-programmable gate arrays (FPGAs). An intermediate alternative between full custom and the previously mentioned array-based approaches is to employ IC design schemes relying on the use of pre-defined cell libraries or generators, in what is called a *cell-based* design approach.

Semi-custom design approaches can be divided into cell-based and array-based ones. Array-based design uses pre-positioned and pre-fabricated transistors and/or other components/structures, which provide the opportunity for the designer to reduce or altogether avoid getting involved in the fabrication process, as when using FPGAs. This approach may penalize achievable performance and power. Array-based is not covered in this work.

Cell-based flows employ pre-designed logic cell libraries, known as *standard cells*, to develop ICs. As Moreira points out in [Mor16]: “Cells are designed at the layout level and implement basic logic functions, including combinational and sequential logic. Note that cells are organized in libraries, which can contain hundreds or thousands of them and the quality of a semi-custom design is a direct function of the quality of the library used to compose it.” Each standard cell is designed, implemented and optimized individually. Optimization criteria encompass sizing and laying out cells for speed, power, resilience, security etc.

Cell-based design greatly reduces design complexity and design time. Implementing asynchronous circuits very often requires the use of specialized components, which are not available in typical commercial cell libraries. Nonetheless, there are few, if any, cell libraries available for those who intend to implement asynchronous circuits using a semi-custom cell-based approach. The lack of commercially available standard cell libraries with dedicated cells for asynchronous design is an acute problem for both the research and commercial deployment of asynchronous techniques. This is accordingly the main motivation to this work.

1.2 Objectives

This End of Term work targeted as main goal the development of an asynchronous standard cell library deemed for application in IC prototyping through fabrication services. To reach the established main goal, some objectives were established:

- The library to develop needed to contain enough cells to support implementing, with a reasonable degree of efficiency,a large spectrum of circuits describable as asynchronous circuits. This implies, for example enabling combination and sequential circuit design to be achievable. Support to some special functionalities were disregarded in this first implementation, though. For example, arbitration within asynchronous circuits may require components like *mutexes*, which will not be considered here for implementation as a cell.
- Full compatibility with some commercial standard cell library in the same fabrication technology is a requirement. This is what enables reducing the library implementation effort and yet supporting the complete design of manufacturable asynchronous ICs.
- The Author dominates the library design flow process at the end of the work.
- The library must be validated with the implementation of some real circuit, even if only to the point preceding the fabrication of some IC.

1.3 Contributions

Of course, the main contribution of this work is the development of the ASCEnD-TSMC180-NCL library, containing 26 cells designed from scratch. The library is fully compatible with the ARM SAGE-X library. Both libraries target the TSMC 180nm bulk CMOS technology.

As a second contribution of the work, the Author dominated every step of the cell and cell library design flow using multiple tools and design frameworks from Cadence and Mentor, two commercial providers of electronic design automation tools for the world semiconductor industry.

A third contribution is the availability of a design environment for using ASCEnD-TSMC180-NCL conjointly with the ARM SAGE-X library to develop asynchronous blocks and whole ICs. By applying these libraries to the development of a digital circuit, the Author demonstrates the compatibility between them.

2. BACKGROUND

This Chapter provides an introduction on some topics required to understand this work. Section 2.1 brings an overview on asynchronous circuit design, showing some of its aspects, like handshake protocols definition and operation, specific cell characteristics associated to some asynchronous design styles etc. Section 2.2 details some of the features of the standard cell-based design process, introducing the background about the cell creation process, from its starting informal logic description to a Spice file through layout generation and design rules verification, until reaching a fully characterized electrical structure for the desired cell.

2.1 Some Asynchronous Design Principles and Techniques

Asynchronous circuits do not rely on the use of a single, global and common time reference (as provided by a global clock signal). In synchronous circuits, all components share a discrete notion of time, as defined by the clock signal distributed throughout the device. Asynchronous circuits are different. As in synchronous circuits, they also employ binary signals that represent information using discrete functions, but time is not discretized. Also, information evolves among circuit modules using local handshake communication instead of all modules marching under the rule of the clock beat.

2.1.1 Handshake Communication

An asynchronous module has often the capacity to communicate with other modules regardless of the speed of its peers. Handshake protocols make this possible, using request and acknowledgment control signals to guarantee the data flow integrity. Figure 2.1 illustrates the general organization of a typical asynchronous pipeline [SF01], also showing an example waveform for a handshake data exchange.

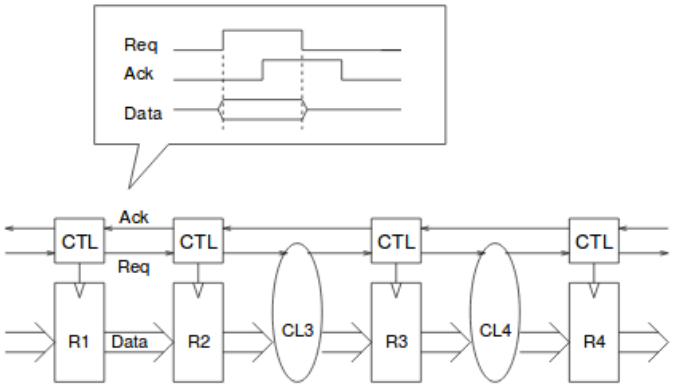


Figure 2.1: A classical asynchronous circuit organization and an instance of a handshake control protocol [SF01].

A handshake channel is where an asynchronous circuit keeps the distinct components synchronized, performing communication. Registers are only loaded where and when needed, and their timing operation is determined by actual circuit delays. A handshake protocol is characterized by two steps (assuming the transmitter initiates communication, which may not be always true): (i) A transmitter module produces a request for communication, announcing data availability; (ii) When ready, the receiver gets the data and acknowledges the request, allowing a new data transmission to take place. Figure 2.2 show a data flow for a linear asynchronous pipeline where handshake signals are abstracted.

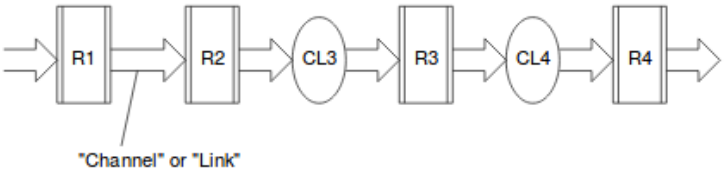
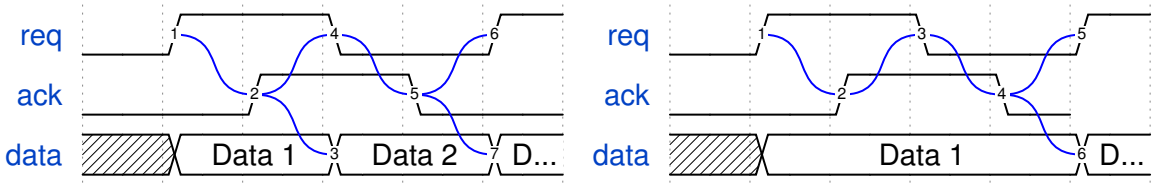


Figure 2.2: An asynchronous data flow representation for a linear pipeline. The handshake between every pair of stages is abstracted in this representation [SF01]. Note that control signals flow in both directions, requests flow in the same sense as data, while acknowledgement signals flow in the reverse direction.

A 2-phase handshake protocol is one where the two steps mentioned above are implemented by single transitions in a control signal or in other equivalent way. Here, new data can be immediately sent after a request is acknowledged. A 4-phase handshake protocol is another protocol that is also commonly used, in which request and acknowledge signals need to be reset (return to their starting values) before new data can be made available and communicated. Figure 2.3 shows instances of a 2-phase and of a 4-phase protocol.



(a) 2-phase handshake protocol. (b) 4-phase handshake protocol.

Figure 2.3: Examples of the two basic types of asynchronous handshake protocols [Sar19].

2.1.2 Quasi Delay Insensitive (QDI) Circuits

Delay insensitive (DI) circuits are those where variations in the values of delays for any of its components (gates, registers etc.) and variations on the delay of any of its wires cannot modify the circuit behavior, i.e. the circuit behavior is absolutely insensitive to delays, provided only that all delays are finite. One of the techniques that facilitates the implementation of DI circuits is the use of DI codes for carrying information between the circuit components [Ver88]. Examples of DI codes are 1-hot, K-out-of-N and Berger codes [Ver88].

Unfortunately, it has been proved that the class of DI circuits is very limited [MD90], and few practical circuits can be implemented that display the DI circuit required properties. The least compromise that can be made to enable the design of circuits that are mostly robust to variations of delays in wires and components relies on the assumption that some wire forks in a circuit are identified as necessarily *isochronic*. This means that the propagation delay from the fork transmitter side to both receiving sides of the fork (or more sides, if the fork goes to more than two distinct places) are the same, or if they differ by some well-defined and *negligible* amount of time. Circuits that are DI except for this compromise are the class of the so-called quasi-delay insensitive (QDI) circuits.

The handshake protocols and channels mentioned in Section 2.1.1 are essential in QDI circuits. In QDI circuits the use of DI codes allow embedding the request signal within the data representation itself. Another technique that improves the delay insensitivity of QDI circuits is, for example, to employ a 4-phase communication protocol coupled to the alternation of valid data and *spacers* in the circuit data wires (a spacer is a special invalid code in a DI scheme, say all wires at 0, to represent the absence of data). Figure 2.4 shows a basic transition diagram for transmitting data on a 1-bit QDI channel.

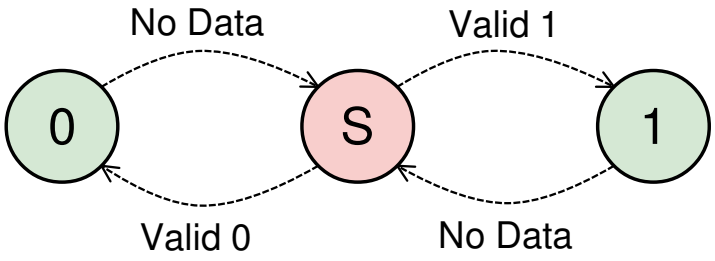


Figure 2.4: The basic transition diagram for transmitting binary data in a QDI channel, where S stands for the spacer, adapted from [MBSC18].

2.1.3 The Null Convention Logic (NCL) Design Technique

Null Convention Logic (NCL), originally proposed by Fant and Brandt [FB96, Fan05], is a semi custom QDI circuit design template that relies on the propagation of spacers during the reset phase of a 4-phase protocol. According to Moreira [Mor16], NCL design has been a subject of research for several groups worldwide and has been used to construct different circuits, especially for low power and small-to-medium sized applications. NCL circuits rely on the existence of special gates, called *threshold* gates or NCL gates. The output of an NCL gate is driven low when all inputs are low. The output is driven high when inputs meet the threshold conditions implied in the specific gate architecture. When the inputs do not fulfill the previous conditions, the gate output keeps its previous value.

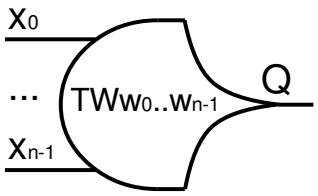
An NCL gate Boolean function expresses the threshold conditions, which often can be computed from a set o weights assigned to each input. Figure 2.5a shows a generic NCL gate, where n is the number of gate inputs, T is the threshold of the gate and each input x_i has a weight w_i.

The gate name reflects its threshold value. For example, a classical 2-input Muller C-Element is equivalent to a 2-input, threshold 2 NCL gate with weight 1 in all inputs. In the convention adopted here, this example gate receives the NCL name 2W211.

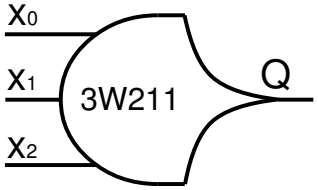
Figure 2.5b shows the 3-input gate 3W211, a 3-input, threshold 3 NCL gate with weight 2, 1 and 1 for the inputs (the convention is to assign weights from the upper inputs to the lower ones, in the order specified in the gate name). Figure 2.5c shows the truth table for this gate.

2.2 Standard Cell-Based Design

Cell-based design uses pre-characterized cell libraries, known as standard cell libraries, to develop IC modules or entire projects. This kind of design relies on a typically technology independent specification of the circuit (say in VHDL or Verilog), a selected technology and one or more cell libraries developed for that technology.



(a) A generic NCL threshold gate.



(b) The 3W211 NCL gate.

(c) The 3W211 NCL gate truth table.

X_0	X_1	X_2	Q_t
0	0	0	0
0	0	1	Q_{t-1}
0	1	0	Q_{t-1}
0	1	1	Q_{t-1}
1	0	0	Q_{t-1}
1	0	1	1
1	1	0	1
1	1	1	1

Figure 2.5: Symbols and example behavior for NCL gates [Sar19].

A standard cell library assumes that cells share a basic set of characteristics, often including: (i) A same height for all cells, to allow easy combination of cells in rectangular rows in the final circuit layout; (ii) Track placement - power and ground rails must be geometrically identical, follow a same orientation (usually horizontal), and be positioned at a same height relative to the cell origin. Also, wires passing over a cell frequently use pre-defined (horizontal and/or vertical) positions, called *tracks*. It is not unusual identify a cell library by the number of separated horizontal metal lines that can pass over the cell. Common examples are 7-track libraries, or 9-track libraries.

To employ a cell library, information must be made available on each cell. This information is organized in views that bring data about: (i) The cell physical structure or layout; (ii) The cell behavior; (iii) The interfaces between the cell and the circuit environment where it is to be used; (iv) The cell electrical characteristics (propagation delay, output delay, power consumption etc.).

2.2.1 The Cell Physical Structure - Layout

The physical structure of a cell is also called its *layout*. A layout is basically a set of rectangles drawn in a given set of technology layers[1]. The cell design must obey a set of rules among rectangles of a same and/or of distinct layers. A process called Design Rule Checking (DRC) verifies if a cell or an entire IC design respects all predefined rules.

DRC is a physical verification process to determine if a cell/IC layout is correct, under the point view of minimal conditions that ensure manufacturability. Each semiconductor process has its own set of rules and defines sufficient margins such that normal variability

[1] Each *layer* corresponds to a given material or physicochemical step used in the IC fabrication process.

in the manufacturing process does not result in IC failure. A rule can be as simple as the minimum width of a wire or the distance between two wires.

The layout view contains information about transistor positions, with their width and height, according to the technology. Metal level interconnections create the desired logic.

2.2.2 Cell Behavior

A cell is designed to work with a pre-defined behavior, usually described in Verilog, a hardware description language. This behavior is combined with that of other cells by automated synthesis processes to produce operational circuits. A cell implements at least a basic function, such as input inversion, or computing Boolean functions such as OR, NOR, AND, NAND, XNOR or XOR. Furthermore, libraries can also contain more complex logic functions, like single or multi-bit adders, multiplexers, flip-flops, encoders, AND-OR-Invert cells, etc.

2.2.3 Interface Between the Cell and its Environment

Libraries gather the so-called abstract views of cells, using a standard format for this, the *Library Exchange Format* (or LEF). The cell abstract view provides information about cell inputs and outputs (pin position, pin size, etc.), routing metals blockages and area usage. Thus, LEF views are in fact an abstraction of the cell layout. They are employed, for example, in the cell placement phase of the physical circuit design process and in the routing phase, for interconnecting cells.

2.2.4 The Cell Electrical Characterization

The cell electrical characterization is usually stored in files that employ the *Liberty* (or LIB) standard format. LIB files define characterization parameters, such as the name of the power rails. They also contain information about power consumption, input and output pins, logic function, input and output capacitances and propagation time of input transitions to output transitions. This information is used for computing, reporting and validating the operation of the design that employs the cell.

2.3 Spice

Spice is a description language useful to model circuits by means of the interconnection of electronic components such as transistors, capacitors, diodes etc. Spice allows the development of circuit topologies at the electric level, being able to express component dimensions, connections and other characteristics, as well as defining input stimuli for exercising the circuit by simulation.

There are several Spice-compatible simulators available, which allow experimenting with circuit inputs (such as input slew rates), outputs (such as the capacitances of output nodes) and internal parameters, such as component dimensions. Spice simulation enables the design of highly optimized small to medium circuits (with typically less than a few thousands transistors).

3. RELATED WORKS

This Chapter introduces relevant works employed in the development of the work proposed here. The Chapter is divided into four sections, Section 3.1 focus on the specific QDI design template to support in this work; Section 3.2 gives the overall cell design process employed here; Section 3.3 presents a development of standard cell library focused in high performance circuits; Section 3.4 approaches the development of a high density standard cell library.

3.1 The SDDS-NCL QDI Design Template

QDI circuits are a class of asynchronous circuits that perform computation on DI-encoded information. A QDI design usually requires less restrictive timing assumptions than other classes of asynchronous design (e.g. bundled-data or speed independent ones). This makes QDI circuits less sensitive to process, voltage and temperature (PVT) variations and ageing.

The library cells developed in this work are destined for use in the design of QDI circuits, more specifically for design templates developed within the scope of the Author's research group. One of these is the SDDS-NCL design template, an enhancement of the NCL template proposed by Moreira [Mor16] and also used in Sartori´s MsC dissertation [Sar19]. Sartori proposed a synthesis flow for QDI circuits called Pulsar, which uses commercial EDA tools along the circuit design process. This method allows designers to use worst-case performance metrics for implementing asynchronous circuit modules. Furthermore, Pulsar allows trading performance, power and area during the circuit optimization phases.

3.2 The ASCEnD Cell Library Implementation Flow

The present work also relies on the cell library development flow described by Moreira in his PhD work [Mor16]. In that Thesis the author explores how to build libraries to support semi custom asynchronous design, improving commercial tools with aids to e.g. better sizing transistors and to characterize asynchronous components. Together with the proposition of a flow for asynchronous cell library design called ASCEnD, Moreira also brought about a fully automated flow for asynchronous circuit design. His techniques describe the optimization of asynchronous design, from design capture to the electric, cell and layout levels. Moreira shows that asynchronous design can be an efficient choice for both low-power and high-performance designs. Given these advantages, he proposes new way of imple-

menting asynchronous design, exploring power, delay and area trade-offs. The Author also presents an exploration of the state of the art in related works in the area of asynchronous project development methods.

3.3 A Proposal of Development for a High Performance Standard Cell Library

The development of high performance standard cell library as proposed by Kotkar [Kot14], has as main objective to increase performance of logic cells satisfying a given specification. The work proposes the development of specific cell library at different drives strengths. The author mentions that designing every logic gate under several different specifications is a very time-consuming process. He points out the possibility of using this high performance cell library to design complex circuits. His techniques describe the benefit of a high performance cell library in highly computing-intensive IC designs, where density can be neglected to meet performance.

3.4 A High Density Standard Cell Library

Melinmani et al. describe the development of a high density standard cell library [MSM19]. The work relies on a traditional library design flow. The library is designed for the technology UMC 180nm CMOS. It is characterized on three corners. The library contains 103 high density, 9-track cell, each cell type presenting from 1 to 5 distinct drive strengths. The library provides layout, schematic, symbol and abstract views. The Author explores the beta ratio calculation, using F03 and calculating the delay in the middle of the chain, a method which according to the authors eliminates slew effects after the 4th or 5th circuit stage.

4. LIBRARY SPECIFICATION AND CELL DEVELOPMENT FLOW

This work presents the development of an NCL cell library to support the design of manufacturable asynchronous circuits that follow a specific QDI template, SDDS-NCL, as proposed by Moreira et al. [MTMC14, Mor16] and later enhanced by Sartori et al. [SWMC19, Sar19]. The library development follows the design flow described in [Mor16], with some differences, due to the evolution of individual techniques and tools composing the flow since its first proposal. The cells developed address the TSMC 180nm bulk CMOS technology. Access to use this technology is granted through the signing of a specific NDA between PUCRS and TSMC, through the EuroPractice service. The reason for choosing this technology is that the Author´s research group has multiple opportunities to employ the latter to perform real IC prototyping, having already successfully designed and tested two operational systems-on-chip (SoCs) in it. To this technology is added the use of a specific library from a third-party vendor, to which the Author´s research group has access. The developed library, called ASCEND-TSMC180-NCL, is fully compatible with the ARM SAGE-X library [ARM08a], henceforth called the *reference library*. Access to use the latter library is granted through the signing of a specific NDA between PUCRS and ARM. The compatibility allows a designer to mix gates from the reference library and the ASCEND-TSMC180-NCL library. This is important to enable the design of complete ICs.

The characteristics of the ASCEND-TSMC180-NCL library are the target of Section 4.1. Section 4.2 presents the library cell development flow.

4.1 The ASCEnD-TSMC180-NCL Library

The complete set of cells in the ASCEnD-TSMC180-NCL library is depicted in Table 4.1. These were developed using the flow described in Section 4.2. Each cell is implemented in one to four drive strengths, in accordance with the available drive strengths of the reference library (XL, X1, X2, X4). These cells, together with several cells from the ARM TSMC 180nm Process 1.8V Sage-X standard cell library [ARM08b] form a basic set to produce pseudo-synchronous [Sar19] SDDS-NCL circuits using the Pulsar flow [Sar19].

The composition of reference library cells and ASCEnD-TSMC180-NCL to produce complete SDDS-NCL circuit modules is as follows:

1. NCL relies on threshold gates, as briefly described in Section 2.1.3. However, an NCL gate with threshold 1 is an ordinary OR gate (present in several flavors in the reference library);

Table 4.1: The complete list of the 26 ASCEND-TSMC180-NCL cells. There are 14 cell classes and up to four drive strengths available.

Cell Class Name	Cell Type	Threshold	Input Weights	Inputs	Drive Strengths
NCL2W11OF2	NCL	2	11	2	XL/X1/X2/X4
NCL3W111OF3	NCL	3	111	3	X4
NCL2W211OF3	NCL	2	211	3	X4
NCL3W211OF3	NCL	3	211	3	X4
RNCL2W11OF2	RNCL	2	11	2+1	X4
SNCL2W11OF2	SNCL	2	11	2+1	X4
INCL2W11OF2	INCL	2	11	2	XL/X1/X2/X4
INCL3W111OF3	INCL	3	111	3	X4
NCLP2W11OF2	NCLP	2	11	2	XL/X1/X2/X4
NCLP3W111OF3	NCLP	3	111	3	X4
NCLP2W211OF3	NCLP	2	211	3	X4
NCLP3W211OF3	NCLP	3	211	3	X4
INCLP2W11OF2	INCLP	2	11	2	XL/X1/X2/X4
INCLP3W111OF3	INCLP	3	111	3	X4

2. SDDS-NCL uses three gate classes besides NCL: (i) NCL inverted counterparts (INCL), where threshold-1 gates are NOR gates; (ii) NCLP gates that follow the RTO protocol not RTZ as in NCL. Here,threshold-1 gates are AND gates; (iii) NCLP inverted counterparts (INCLP), where threshold-1 gates are NAND gates;

3. As a consequence of the previous two items and of the chosen full compatibility of the involved libraries, ASCEnD-TSMC180-NCL need not contain any threshold-1 gates. Accordingly, all cells ASCEnD-TSMC180-NCL are sequential gates with some degree of hysteresis, functionality absent in commercial cell libraries;

4. It is often necessary, during digital circuit implementation, to generate storage devices that can be initialized. Thus, a minimum ensemble of gates with set or/and reset control is necessary in ASCEnD-TSMC180-NCL. Note that ordinary flops and latches from the reference library have no use in NCL or SDDS-NCL design.

Assuming the above information on how cells from the two libraries are composed or excluded from use, it is then possible to interpret the data in Table 4.1. Every specific instance of a cell has a name structured according to the following Backus-Naur Form (BNF): **[R|S][I]NCL[P]<T>W<ws>OF<ins>X<L|1|2|4>**. Here, elements between square brackets ([ ]) are optionally present, vertical bars (|) represent choices and elements between angle brackets (<>) are mandatory in the name, while letters outside all mentioned brackets are mandatory and present as themselves in the name. The latter correspond to type designators and/or field separators. **<T>** is a number representing the threshold of the gate, **<ws>** is the set of natural number weights, one for each gate input, **<ins>** is the number of inputs of the gate, and the field after the **X** letter represents the cell instance drive strength. For example, the cell classes NCL2W11OF2 and NCL3W111OF3 are respectively 2- and 3-input

C-Elements (conventional RTZ gates). This notation extends the generic NCL gate naming presented in Section 2.1.3.

One feature of the library is that some cells have the property that their functional behavior can be interpreted in different forms by naming their pins differently. This feature enables that some cell pairs share a same layout. Analysis conducted here showed that the 26 cells in the ASCEnD-TSMC180-NCL library only require 14 distinct cell layouts. For example, cells NCLP2W211OF3 and NCL2W211OF3 can be used as a settable and as a resetable C-element, respectively. The latter interpretations allow them to be employed as components of registers. In addition, to use these cells in an SDDS-NCL design environment, it is necessary to develop cells in complementary pairs, as explained in detail, e.g. in [MTMC14]. Such pairs are determined through the concept of *virtual functions* [MTMC14].

Besides the functional characteristics, cells can be differentiated by their *strength*, the relative capacity of a cell to drive its output, using *Xi*. The bigger the value of *i*, the stronger the cell. An *X*1 cell can drive a certain output capacitance with a certain delay. However, an *X*4 cell can drive a 4 times larger capacitance with the same delay as cell *X*1. The *XL* designator corresponds to a drive with nominally half the drive strength of *X*1, *L* standing for *low drive strength*. In this work, cell output buffers are sized to agree with the drive strength definition defined in the reference library (ARM TSMC 180nm Process 1.8V Sage-X standard cell library [ARM08b]).

Table 4.2 describes the functionality for each of the 12 cell classes that are used to build combinational circuits (all cells, except those with set or reset pins). Functionality is described in terms of the cell sequential behavior (using its characteristic function) and by means of the cell virtual function (used by commercial synthesis tools to manipulate the cell). Note that an NCL gate virtual function is a function that produces 1 for every input combination (and only for these) that makes the NCL gate producing 1. Similar but not identical observations hold for INCL, NCLP and INCLP gates, see [Sar19] for more on this. More formally, a virtual function or *vfunction* is a Boolean function associated with the NCL, NCLP, INCL or INCLP gates, which represents its support gate. Vfunctions *f* are defined as follows [SWMC19]:

1. if the support gate of *f* is an NCL gate A, the ON-set of *f* is the same as the ON-set of A. The OFF-set of *f* comprises all other n-input patterns;

2. if the support gate of *f* is an NCLP gate B, the OFF-set of *f* is the same as the OFF-set of B. The ON-set of *f* comprises all other n-input patterns;

3. if the support gate of *f* is an INCL gate C, the OFF-set of *f* is the same as the OFF-set of C. The ON-set of *f* comprises all other n-input patterns;

4. if the support gate of *f* is an INCLP gate D, the ON-set of *f* is the same as the ON-set of D. The OFF-set of *f* comprises all other n-input patterns.

If the support gate of *f* is of type NCL or NCLP, f is a positive vfunction. Otherwise, *f* is a negative vfunction.

Table 4.2: A list of the implemented 12 combinational cell classes, with their respective characteristic functions and virtual functions. A, B etc are cell inputs and Y is the cell output.

Gate Name	Characteristic Function	Virtual Function
NCL2W11OF2	$(A * B) + Y * (A + B)$	$A * B$
NCL3W111OF3	$(A * B * C) + Y * (A + B + C)$	$A * B * C$
NCL2W211OF3	$B * C + Y * (B + C) + A$	$A + B * C$
NCL3W211OF3	$A * (B + C) + Y * (A + B + C)$	$A * (B + C)$
INCL2W11OF2	$!((A * B)+!Y * (A + B))$	$!(A * B)$
INCL3W111OF3	$!((A * B * C)+!Y * (A + B + C))$	$!(A * B * C)$
NCLP2W11OF2	$(A * B) + Y * (A + B)$	$A + B$
NCLP3W111OF3	$(A * B * C) + Y * (A + B + C)$	$A + B + C$
NCLP2W211OF3	$(B * C + Y * (B + C)) * A$	$A * (B + C)$
NCLP3W211OF3	$A * B * C + Y * (A + B * C)$	$A + B * C$
INCLP2W11OF2	$!((A * B)+!Y * (A + B))$	$!(A + B)$
INCLP3W111OF3	$!((A * B * C)+!Y * (A + B + C))$	$!(A + B + C)$

An observation regarding the cell composition of library ASCEnD-TSMC180-NCL is that all possible threshold functions depending on up to three inputs can be produced with just one library gate, with a single exception, the NCL2W111OF3 gate [Fan05]. No version of this gate could be developed in the time available to complete this work. Its implementation is a recommended future work, to make the library functionally complete for functions with up to three inputs. Also, an attentive reader will note in Table 4.1 that the current state of ASCEnD-TSMC180-NCL could benefit from a larger diversity of drive strengths for many of the cells, which is another useful future work. Several publications on NCL mention the availability of functions with up to four inputs [Fan05]. Although not necessary to implement circuits in general, expanding library ASCEnD-TSMC180-NCL to contain 4-input cells could be useful to enable more flexibility during circuit synthesis. Note however that 4-input functions can be cumbersome. For ultra low power circuits operating under deep voltage scaling (e.g. in near- and sub-threshold regimes) 4-input functions are typically not used.

4.2 ASCEnD-TSMC180-NCL Cell Development Flow

Developing a cell from scratch is an activity contemplating multiple steps, some of which imply iterative refinements. Linearizing these steps, it is possible to divide tasks associated with cell development into eight steps: (i) functionality design; (ii) schematic view capture; (iii) transistor sizing; (iv) layout view generation; (v) layout verification; (vi) layout extraction; (vii) characterization view; (viii) abstract view generation. The four steps with the word “view” in their names (ii, iv, vii and viii) produce each a part of the cell description that

together form the complete information set about that cell in the library. The distinct views are used along IC development by several design and verification tools.

Figure 4.1 details the cell development flow, which operation is discussed in the next three sections.

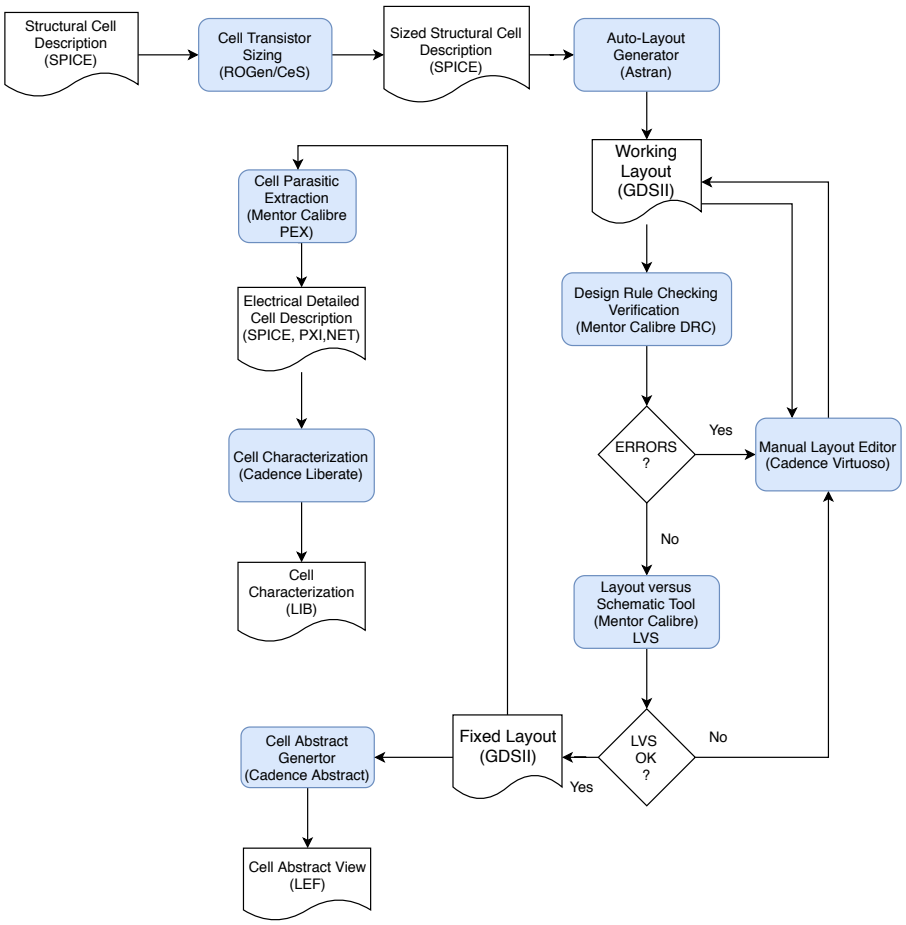


Figure 4.1: A simplified flow diagram representing the cell development process used in this work.

4.2.1 Cell Transistor Sizing

As mentioned before, a library may contain multiple driving strengths, which indicate the relative capability of a gate to drive an output load. At the layout level, different drive strengths are obtained by transistor *folding* or *fingering*. For example, “X4” indicates four folds. The reference library also provides a half-fold configuration identified by the suffix “XL”.

For each cell, the driving strength defines how to dimension the cell output buffer. These are often inverters dimensioned according to inverters of corresponding driving strength from the reference library. Figure 4.2a depicts a cell schematic with an output buffer for a “X4” driving strength cell.

Transistor sizing in this work relies on the use of the ROGen/CeS in-house tools. ROGen/CeS execution is parameterized by an input configuration file. This file is prepared based on the technology under use, on the library compatibility issues and on the definition of ranges for the variable amounts employed by the programs. Given that a previous effort by the GAPH group already generated such a configuration file for the TSMC 180nm technology, when proposing the ASCEnD-TSMC180-Velo library [Gua17], this work chose to employ this configuration as is, after careful consideration of its contents. The starting point for sizing cell transistors is a Spice schematic derived from the behavioral specification of the cell. In this schematic the width of output, state-holding and feedback transistors are fixed to pre-determined values and the transistors taking part on the set and reset logic of the gate are subject of transistor sizing. This is a simplification of the transistor sizing process, employed by the ROGen tool. The parametric variable `pparam` is assigned to the width of PMOS transistors subject to sizing. Similarly, the parametric variable `nparam` is assigned to the width of NMOS transistors subject to sizing. The length for all cell transistors is kept fixed at the minimum value, another simplification adopted by ROGen. ROGen and CeS are in-house software tools of the GAPH group, used to perform the transistor sizing process and to help the user to pick the best size options. ROGen generates Spice simulation decks where each instance of a sized cell is arranged in a ring oscillator. This simulation deck is used to explore a range for sizing parameters `pparam` and `nparam`. The ring oscillator is simulated for each combination of values for sizing parameters. Power and timing results are then collected from simulations. Next, CeS analyses the power and timing results and selects the best sizing parameters, according to a user-defined cost function. The output of CeS is a Spice schematic with all transistors sized. An example output of CeS is depicted in Figure 4.2b.

4.2.2 Layout Place and Route

The layout is generated from the new schematic with Astran [ZRM+14], once the sizing is completed. An example layout produced by Astran is depicted in Figure 4.3. This generated layout does not always respect the target technology abutment and design rules. This occurs because Astran offers little flexibility to parameterize its layout generation process.

However, it is possible to manually correct the layout generated by Astran. Layout correction follows a loop where design rules are checked using the Calibre DRC tool and if rules are violated the layout is manually fixed with the Cadence Virtuoso layout editor. The loop goes on until no design rule violations are left.

When no further violations are found by the DRC tool, the equivalence between the layout and the schematic is checked. The Layout versus Schematic (LVS) tool [Men19],

```
.SUBCKT INCL2W211OF3X4 A B C QN GND VDD
*.pininfo A:I B:I C:I QN:O GND:G VDD:P
*SET/RESET logic
MPS00 VDD  A pl00 VDD pch W=pparam L=0.18u
MPS01 pl00 B pl01 VDD pch W=pparam L=0.18u
MPS02 pl01 C PREQ VDD pch W=pparam L=0.18u
MNS01 PREQ C nl01 GND nch W=nparam L=0.18u
MNS02 nl01 B GND  GND nch W=nparam L=0.18u
MNS03 PREQ A GND  GND nch W=nparam L=0.18u
*FeedbacK INV + HOLD1/HOLD1
MPF00 FBP  IQ PREQ VDD pch W=0.42u L=0.18u
MPF01 FBP  A  FBP0 VDD pch W=0.42u L=0.18u
MPF02 VDD  B  FBP  VDD pch W=0.42u L=0.18u
MPF03 VDD  C  FBP  VDD pch W=0.42u L=0.18u
MNF00 FBN  IQ PREQ GND nch W=0.42u L=0.18u
MNF01 FBN  A  GND  GND nch W=0.42u L=0.18u
MNF02 FBN  B  GND  GND nch W=0.42u L=0.18u
MNF03 FBN  C  GND  GND nch W=0.42u L=0.18u
*Output BUFF
MPI00 VDD PREQ IQ VDD pch W=1.44u L=0.18u
MPI01 VDD IQ   QN VDD pch W=3.52u L=0.18u
MNI00 GND PREQ IQ GND nch W=0.96u L=0.18u
MNI01 GND IQ   QN GND nch W=2.4u L=0.18u
*Transistors count: NMOS 8 PMOS 8 TOTAL 16
*.SCALE meter
*.ROGen:THR 2
*.ROGen:IN 3
*.ROGen:DRV X4
*.ROGen:PIN in in in out gnd vdd
*.ROGen:PTC RTZ
*.ROGen:INV 1
*.ROGen:CONF NONE
*.ROGen:RST 0
*.ROGen:SET 1
.ENDS
```

(a) The cell SPICE description, pre-ROGen.

```
.SUBCKT INCL2W211OF3X4 A B C QN GND VDD
*.pininfo A:I B:I C:I QN:O GND:G VDD:P
*SET/RESET logic
MPS00 VDD  A pl00 VDD pch W=0.56u nf=1 L=0.18u
MPS01 pl00 B pl01 VDD pch W=0.56u nf=1 L=0.18u
MPS02 pl01 C PREQ VDD pch W=0.56u nf=1 L=0.18u
MNS01 PREQ C nl01 GND nch W=0.44u nf=1 L=0.18u
MNS02 nl01 B GND  GND nch W=0.44u nf=1 L=0.18u
MNS03 PREQ A GND  GND nch W=0.44u nf=1 L=0.18u
*FeedbacK INV + HOLD1/HOLD1
MPF00 FBP0 IQ PREQ VDD pch W=0.42u L=0.18u
MPF01 FBP  A  FBP0 VDD pch W=0.42u L=0.18u
MPF02 VDD  B  FBP  VDD pch W=0.42u L=0.18u
MPF03 VDD  C  FBP  VDD pch W=0.42u L=0.18u
MNF00 FBN  IQ PREQ GND nch W=0.42u L=0.18u
MNF01 FBN  A  GND  GND nch W=0.42u L=0.18u
MNF02 FBN  B  GND  GND nch W=0.42u L=0.18u
MNF03 FBN  C  GND  GND nch W=0.42u L=0.18u
*Output BUFF
MPI00 VDD PREQ IQ VDD pch W=1.44u L=0.18u
MPI01 VDD IQ   QN VDD pch W=3.52u L=0.18u
MNI00 GND PREQ IQ GND nch W=0.96u L=0.18u
MNI01 GND IQ   QN GND nch W=2.4u L=0.18u
*Transistors count: NMOS 8 PMOS 8 TOTAL 16
*.SCALE meter
*.ROGen:THR 2
*.ROGen:IN 3
*.ROGen:DRV X4
*.ROGen:PIN in in in out gnd vdd
*.ROGen:PTC RTZ
*.ROGen:INV 1
*.ROGen:CONF NONE
*.ROGen:RST 0
*.ROGen:SET 1
.ENDS
```

(b) The cell SPICE description, post-ROGen.

Figure 4.2: Pre- and post-sizing descriptions for INCL2W2110F3x4 cell.

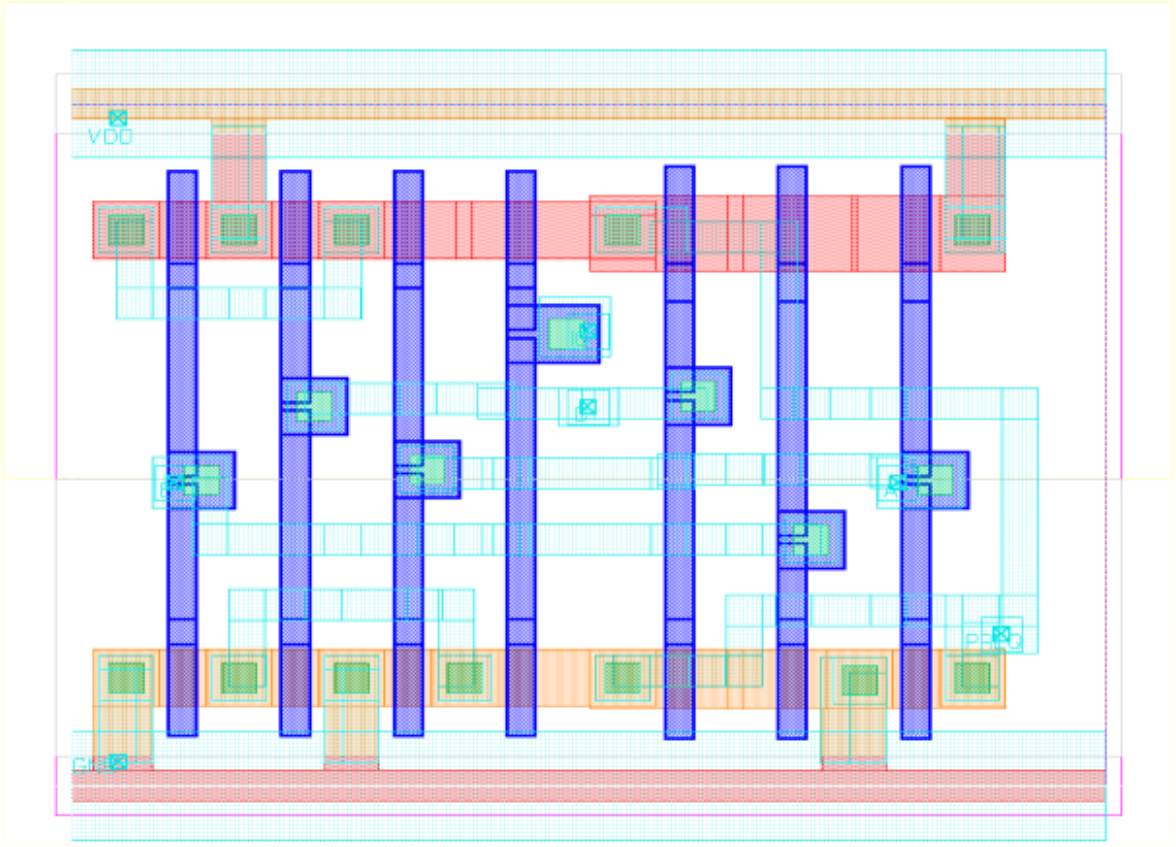


Figure 4.3: Astran output for cell INCL2W2110F3x4.

requires a layout with dimensioned transistors and no design rule violations. LVS checks the

equivalence of the layout and schematic descriptions. If the LVS tool accuses inconsistencies between the layout and the schematic, the designer has to fix the layout to meet the schematic. After correcting the layout, the designer needs to iterate the DRC and equivalence verification steps, until reaching a fully error-free layout. Notice that both design rules and equivalence correction steps might require multiple iterations until no errors are reported by neither the LVS nor the DRC tool. Once both tools report no violations on a given layout, the latter is deemed corrected and the flow moves on.

Furthermore, some rules must be followed to maintain compatibility with the reference library. Among these rules, one states that the height of each cell group should be the same as cells in the reference library. The width of each cell must be integer multiple of a defined *grid size* value. This is so because during the placement process cells are instantiated side by side on a *placement grid*. When measurements of height, width, and boundaries of the cell group are not compatible, it is impossible to make the placement and route of the circuit using these cells in association with those of the reference library. Besides the placement grid, the cell input and output pins are advised to align to a pre-defined *routing grid*. However, this is just a guideline and pins unaligned with the routing grid may connect correctly, albeit the routing process might be slower due to the introduced added complexity. According to the documentation of the reference library, pins could be placed at either Metal1 or Metal2 layers. However, cells developed in this work employ only Metal1 pins.

4.2.3 Cell Characterization and Abstract View Generation

The process of characterization of a library is crucial in its development. Through it one can obtain information such as the capacitance of pins, the cell leakage, cell delays, and cell power parameters. A set of rules must be followed to guarantee full compatibility with the reference library though. The SAGE-X ARM cell library has a set of characteristics such as propagation delay, basic drive strengths, transition times definition, etc.

The SAGE-X manual [ARM08a] states that the propagation delay through a cell is the sum of the intrinsic delay, the load-dependent delay, and the input-slew dependent delay. Delays are defined as the time interval between a transition in some cell input and a corresponding transition in the cell output. The library manual defines that signal rise transitions are detected when the signal voltage rises above 50% of the supply voltage. Similarly, it defines that a fall transition is detected when the signal falls bellow 50% of the supply voltage. Rise and fall transitions are depicted in Figure 4.4. Besides propagation delay, another property of signals captured during characterization is the *transition time*, also known as *slew*. This property is defined as the time interval between a signal crossing

from 10% to 90% of the supply voltage for a rising signal, and crossing from 90% to 10% of the supply voltage for a falling signal, as Figure 4.5 illustrates.

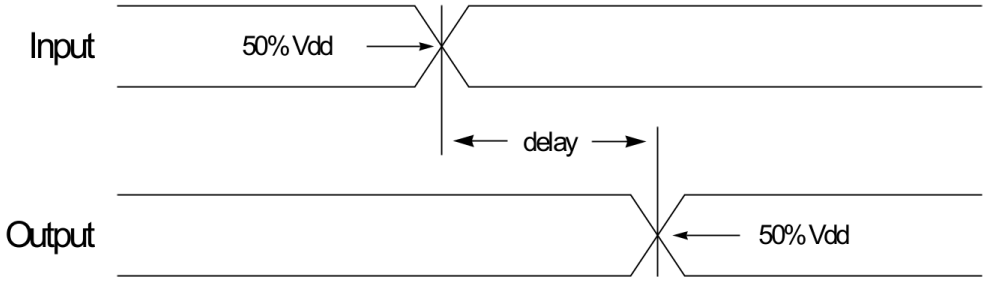


Figure 4.4: Propagation delay at 50/50, adapted from [ARM08a] .

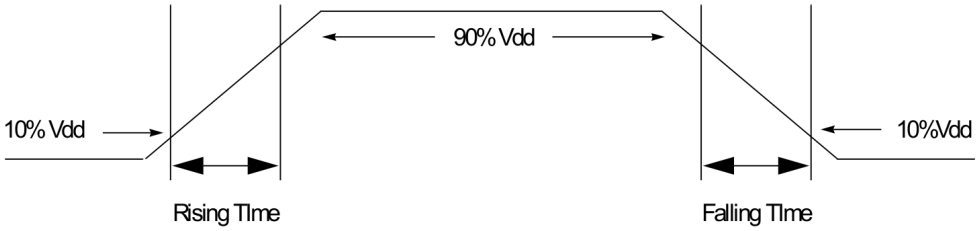


Figure 4.5: Signal transition times definition, adapted from [ARM08a].

For each gate the input transition times and the output capacitance affect the timing and power behavior of the cell. These timing characteristics are captured in a standardized file format called Liberty. This file describes the timing and power behavior of each cell through a set of tables. They describe the timing and power behavior of the cell under different input slews and different output capacitances. The Liberty file is used during synthesis to select the proper cell to implement the design logic function. It is also used during sign-off to verify if the design meets the timing requirements. These files are the result of the characterization process, described in Section 2.2.4. In this work, the characterization is performed using the Cadence Liberate [Cad19] tool. Liberate performs a series of Spice simulations on the gate netlist and generates a set of tables describing the propagation delay, output transition and power consumption figures for the cell. Environmental conditions such as temperature, supply voltage and process variations affect the characterized parameters. For this reason, the proposed library is characterized in three different corners, slow, nominal and fast, each with their respective process, temperature and supply voltage characteristics, as show in Table 4.3.

In order to improve the quality of the resulting characterization data, the netlist used for simulation by Liberate must contain parasitic capacitances and resistances. These are unintended side-effects of how transistors and wires are laid out and interconnected in

Table 4.3: A list of the characterized corners in the library.

Corner	Voltage(V)	Temperature(T)
Slow	1.62V	125ºC
Nominal	1.8V	25ºC
Fast	1.92V	-40ºC

the cell. A Spice netlist containing these parasitic capacitances and resistances is extracted using a Cell Parasitic Extraction (PEX) program. This extracted Spice netlist is a replacement for the sized schematic that captures more precisely (under the electrical point of view) the cell behavior.

Another important file to enable the use of a cell in synthesis flows is the `LEF` file, containing the cell abstract view. This file contains information about the cell boundary, I/O pins and metal obstructions. This is necessary for automatic layout tools (placement and routing). With this view tools know where to route layers over the cell without violating geometrical design rules and without producing undesired connections. The abstract view is extracted and exported using the *Abstract* tool, included in the Cadence Virtuoso design suite.

5. ASCEND-TSMC180-NCL VALIDATION

To validate a cell library, it is required to create a circuit that uses the developed cells. The circuit proposed for achieving this goal is a 32-bit pipeline adder with 8 inputs. The design is depicted in Figure 5.1. This circuit was implemented using cells from the developed and reference libraries together, to test their compatibility. A pipeline adder was chosen due to its size and complexity, implying that it instantiates a variety of cells multiple times. This increases the opportunity that possible abutment and grid rules violations manifest as DRC errors, enabling to test the compatibility between ASCEND-TSMC180-NCL and the reference library.

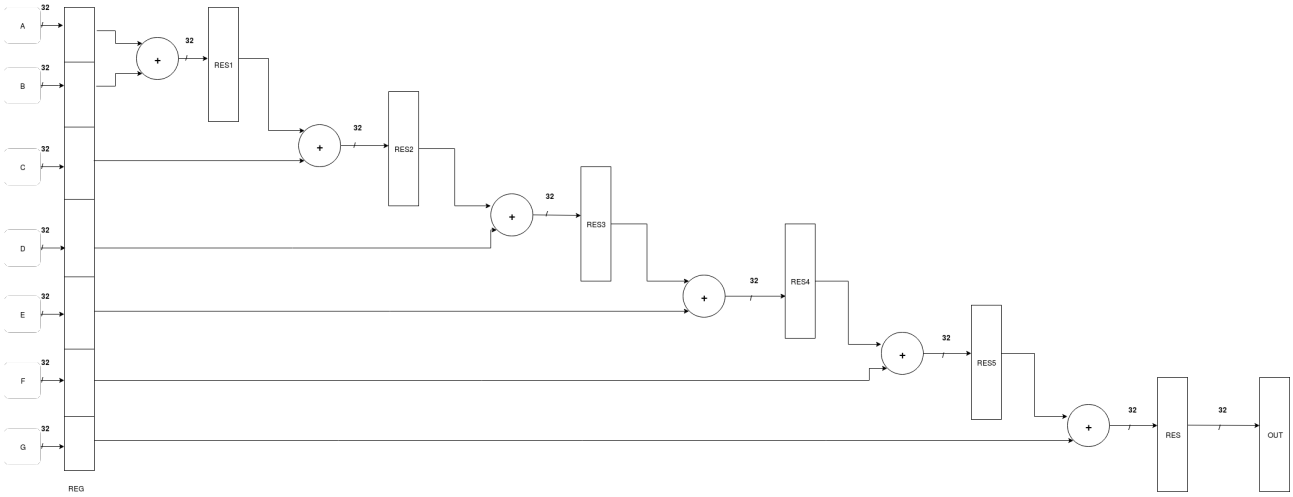


Figure 5.1: The schematic of the pipeline adder.

The circuit was designed and synthesized using the Pulsar flow proposed in [SWMC19, Sar19]. It produces an SDDS-NCL asynchronous QDI circuit from a synchronous description. The RTL-like description of the pipeline adder appears in Listing 5.1. The synthesis flow was adapted to incorporate the cells from the developed and reference libraries. Logic synthesis was performed with a cycle-time constraint of 20 ns on the slow characterization corner, at 125 °C and 1.68 V. Note that using the slow corner for synthesis is standard industrial design practice to obtain a circuit guaranteed to operate under worst-case conditions. The gate count per library for the synthesized circuit netlist is depicted in Table 5.1.

Listing 5.1: Verilog description of the proposed pipeline adder.

```
module adder(a, b, c, d, e, f, g, out, clk);
        input wire [31:0] a, b, c, d, e, f, g;
        output reg [31:0] out;
        input wire clk;

        reg [31:0] reg_a, reg_b, reg_c, reg_d, reg_e, reg_f, reg_g;
```

```
    reg [31:0] res_1, res_2, res_3, res_4, res_5, res;

    always @(posedge clk) begin
        reg_a <= a;
        reg_b <= b;
        reg_c <= c;
        reg_d <= d;
        reg_e <= e;
        reg_f <= f;
        reg_g <= g;
        res_1 <= reg_a + reg_b;
        res_2 <= reg_c + res_1;
        res_3 <= reg_d + res_2;
        res_4 <= reg_e + res_3;
        res_5 <= reg_f + res_4;
        res <= reg_g + res_5;
        out <= res;
    end
endmodule
```

Table 5.1: List of total gate instances used in the circuit and gate percentages by library.

Library	Instances	Area	Instances %
ASCEND_TSMC180_NCL	4123	188590.248	58.5
sage-x_tsmc_cl018g_rvt	2927	33071.069	41.5

From the 26 cells of the ASCEnd-TSMC180-NCL library, only 20 were employed in the adder implementation, as detailed in Table 5.2. A large number of cells from the reference library is used, because (as mentioned before) gates with threshold 1 correspond to cells available in the reference library (ANDs, NANDs, ORs and NORs). It can be inferred that this design validates ASCEnd-TSMC180-NCL and its compatibility with the reference library. As can be seen, 6 of the ASCEnd-TSMC180-NCL cells were not employed in the adder design. These are: NCL2W11OF2X1, NCL2W11OF2X4, SNCL2W11OF2X4, NCLP2W11OF2X1, NCLP2W11OF2X4, INCLP2W11OF2X1. These cells were not used because of several particular reasons. For example, in the case of SNCL2W11OF2X4, there is no set control signal in the circuit description. As for the remaining cells, all cell types were used, but some drive strengths of some cells were not necessary. The circuit presents a large area in comparison to a similar synchronous pipeline adder circuit. This increase is in part justifiable by the use of dual-rail codes. A dual-rail circuit employs three wires to implement each wire of the equivalent single-rail circuit, two wires carry the dual-rail encoded data and one wire implements the acknowledgment for handshake control. This also implies

that the dual-rail expanded circuit has 3-fold the number of ports compare to its single-rail counterpart, two ports for the dual-rail encoded data and one port for the acknowledgment signal.

Table 5.2: List of instantiated gates used in the pipeline adder circuit. Includes details on the number of instances of each cell and the total area taken by this cell. The last column indicates the library from where the cell is taken.

Gate	Instances	Area	Library
AND2X1	7	93.139	sage-x_tsmc_cl018g_rvt
AND2X2	10	133.056	sage-x_tsmc_cl018g_rvt
AND2X4	2	33.264	sage-x_tsmc_cl018g_rvt
AND2XL	42	558.835	sage-x_tsmc_cl018g_rvt
AND3X1	4	66.528	sage-x_tsmc_cl018g_rvt
AND3X2	5	89.160	sage-x_tsmc_cl018g_rvt
AND3X4	3	59.875	sage-x_tsmc_cl018g_rvt
AND3XL	4	66.528	sage-x_tsmc_cl018g_rvt
BUFX1	12	159.667	sage-x_tsmc_cl018g_rvt
BUFX2	5	66.528	sage-x_tsmc_cl018g_rvt
BUFXL	42	558.835	sage-x_tsmc_cl018g_rvt
CLKBUFX2	9	119.750	sage-x_tsmc_cl018g_rvt
CLKBUFX3	103	1370.477	sage-x_tsmc_cl018g_rvt
CLKBUFX4	2	33.264	sage-x_tsmc_cl018g_rvt
CLKBUFXL	7	93.139	sage-x_tsmc_cl018g_rvt
CLKINVX1	201	2005.819	sage-x_tsmc_cl018g_rvt
CLKINVX2	92	918.086	sage-x_tsmc_cl018g_rvt
CLKINVX4	5	49.896	sage-x_tsmc_cl018g_rvt
CLKINVXL	22	292.723	sage-x_tsmc_cl018g_rvt
INCL2W11OF2X1	26	1297.296	ASCEND_TSMC180_NCL
INCL2W11OF2X2	33	1317.254	ASCEND_TSMC180_NCL
INCL2W11OF2X4	23	994.594	ASCEND_TSMC180_NCL
INCL2W11OF2XL	219	8747.779	ASCEND_TSMC180_NCL
INCL3W111OF3X4	108	5388.768	ASCEND_TSMC180_NCL
INCLP2W11OF2X2	111	4430.765	ASCEND_TSMC180_NCL
INCLP2W11OF2X4	56	2421.619	ASCEND_TSMC180_NCL
INCLP2W11OF2XL	316	12613.709	ASCEND_TSMC180_NCL
INCLP3W111OF3X4	164	8182.944	ASCEND_TSMC180_NCL
INVX1	67	445.738	sage-x_tsmc_cl018g_rvt
INVX12	26	1124.323	sage-x_tsmc_cl018g_rvt
INVX2	19	189.605	sage-x_tsmc_cl018g_rvt
INVX3	1	13.306	sage-x_tsmc_cl018g_rvt

Table 5.2: List of instantiated gates used in the pipeline adder circuit. Includes details on the number of instances of each cell and the total area taken by this cell. The last column indicates the library from where the cell is taken (continued).

Gate	Instances	Area	Library
INVX4	3	39.917	sage-x_tsmc_cl018g_rvt
INVXL	867	5767.978	sage-x_tsmc_cl018g_rvt
NAND2X1	37	369.230	sage-x_tsmc_cl018g_rvt
NAND2X2	36	598.752	sage-x_tsmc_cl018g_rvt
NAND2X4	4	93.139	sage-x_tsmc_cl018g_rvt
NAND2XL	113	1127.650	sage-x_tsmc_cl018g_rvt
NAND3X1	3	39.917	sage-x_tsmc_cl018g_rvt
NAND3X2	9	209.563	sage-x_tsmc_cl018g_rvt
NAND3X4	2	66.528	sage-x_tsmc_cl018g_rvt
NAND3XL	6	79.834	sage-x_tsmc_cl018g_rvt
NCL2W11OF2X2	69	2524.738	ASCEND_TSMC180_NCL
NCL2W11OF2XL	636	25387.738	ASCEND_TSMC180_NCL
NCL2W211OF3X4	353	17613.288	ASCEND_TSMC180_NCL
NCL3W111OF3X4	261	13022.856	ASCEND_TSMC180_NCL
NCL3W211OF3X4	394	19659.024	ASCEND_TSMC180_NCL
NCLP2W11OF2X2	117	4281.077	ASCEND_TSMC180_NCL
NCLP2W11OF2XL	101	4031.597	ASCEND_TSMC180_NCL
NCLP2W211OF3X4	119	5937.624	ASCEND_TSMC180_NCL
NCLP3W111OF3X4	76	3792.096	ASCEND_TSMC180_NCL
NCLP3W211OF3X4	45	2245.320	ASCEND_TSMC180_NCL
NOR2X1	267	2664.446	sage-x_tsmc_cl018g_rvt
NOR2X2	215	3575.880	sage-x_tsmc_cl018g_rvt
NOR2X4	17	395.842	sage-x_tsmc_cl018g_rvt
NOR2XL	100	997.920	sage-x_tsmc_cl018g_rvt
NOR3X1	10	133.056	sage-x_tsmc_cl018g_rvt
NOR3X2	26	605.405	sage-x_tsmc_cl018g_rvt
NOR3X4	10	332.640	sage-x_tsmc_cl018g_rvt
NOR3XL	1	13.306	sage-x_tsmc_cl018g_rvt
OR2X1	45	598.752	sage-x_tsmc_cl018g_rvt
OR2X2	33	439.085	sage-x_tsmc_cl018g_rvt
OR2X4	74	1476.922	sage-x_tsmc_cl018g_rvt
OR2XL	336	4470.682	sage-x_tsmc_cl018g_rvt
OR2X1	3	59.875	sage-x_tsmc_cl018g_rvt
OR2X2	2	39.917	sage-x_tsmc_cl018g_rvt
OR2X4	3	89.813	sage-x_tsmc_cl018g_rvt
OR2XL	15	249.480	sage-x_tsmc_cl018g_rvt

Table 5.2: List of instantiated gates used in the pipeline adder circuit. Includes details on the number of instances of each cell and the total area taken by this cell. The last column indicates the library from where the cell is taken (continued).

Gate	Instances	Area	Library
RNCL2W11OF2X4	896	44706.816	sage-x_tsmc_cl018g_rvt
TOTAL	7050	221661.317	

The circuit was placed and routed using Cadence Innovus, the resulting layout is depicted in Figure 5.2. Innovus places the cells from the aforementioned libraries and routes wires, connecting gates according to the netlist constructed on the logical synthesis. The layout implemented by Innovus is depicted in Figure 5.2. Innovus is able to verify interconnection DRC, connectivity and antenna violations at a global level using the cells abstract view. This verification asserts that the cells were correctly placed in the grid, and that the router successfully reached the cell pins. Once it was deemed cleaned by Innovus, the design was exported into Virtuoso for further validation. On Virtuoso, the cells layout views were integrated into the circuit layout yielding a complete view of layout. Mentor Calibre was used to check DRC violations on the complete layout containing the placed cells. This checks for possible DRC violations between placed cells in all layers, thus validating the abutment rules conformance.

In order to further validate the cell library, the adder design was tested by electrical simulation. This process validates the integrity of the circuit logic, asserting the electrical compatibility of ASCEnd-TSMC180-NCL and reference libraries. The electrical simulation was performed using an analogue-mixed-signal (AMS) simulation environment. It comprises: a Spice netlist extracted from the the layout; a SPEF file containing the parasitic capacitances of wires in the layout; a transistor level netlist of all cells from both libraries; a transistor model for the technology supplied by the foundry; and a digital testbench to provide stimuli and check computational results. The digital testbench written in SystemVerilog stimulates the circuit, providing data for computation and consuming the results output by the circuit. It also verifies the computation result in order to validate the correct logical operation of the circuit. A waveform showing the acknowledgment signals at the first bit of each input and output is depicted in Figure 5.3. As previously discussed on Section 2.1, the acknowledgment signals coordinates the handshake process. Through the behavior of the acknowledgment signals, it is possible to observe that the circuit consumes data and produces results that is readily consumed by the simulated environment. The SystemVerilog testbench asserted that all observed computations were correct. These results demonstrate that the circuit operates correctly.

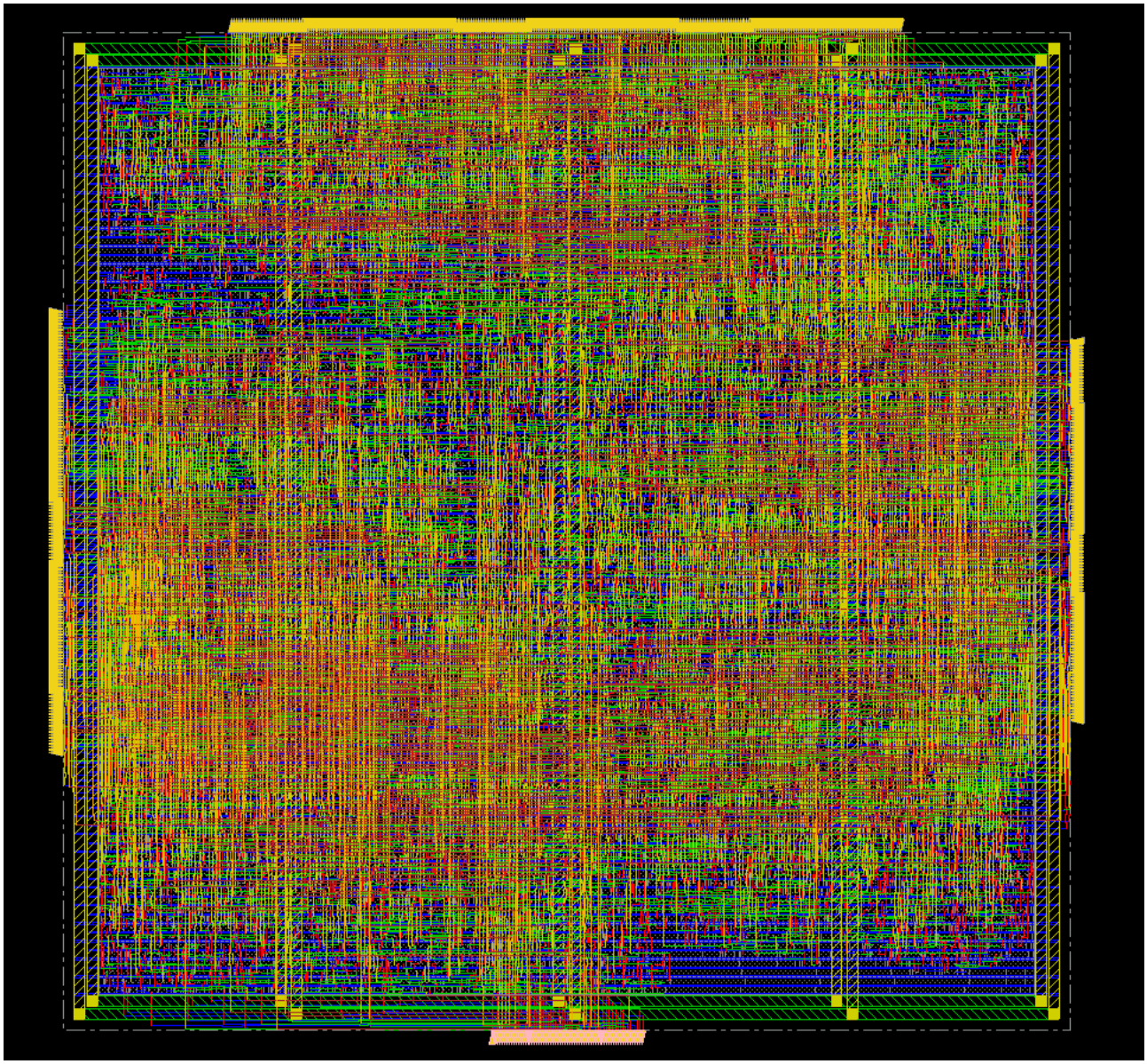


Figure 5.2: The Innovus view of the developed circuit.

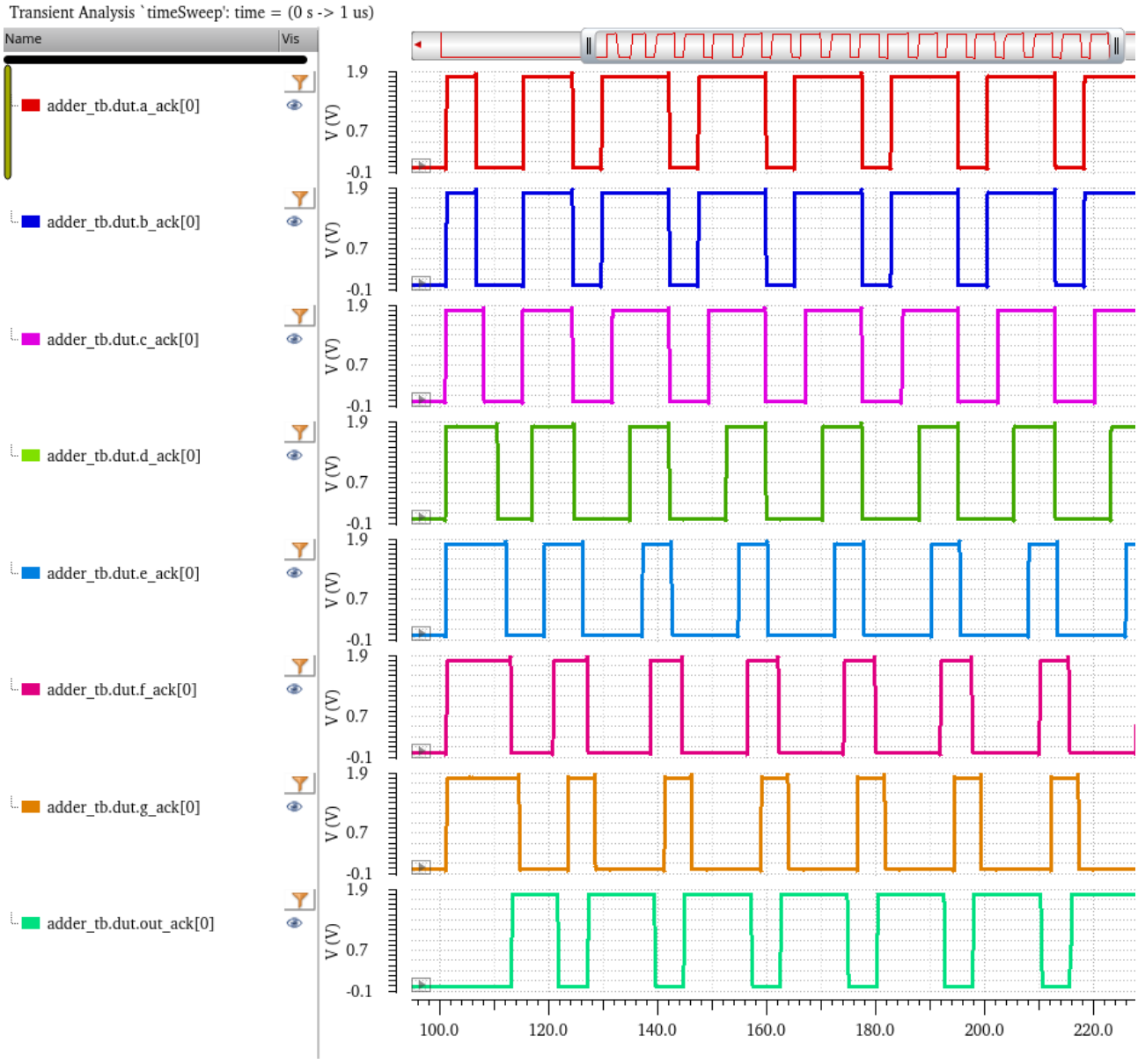


Figure 5.3: Waveform showing the ack signals switching activity, captured from the adder analog simulation.

6. CONCLUSIONS AND FUTURE WORK

Standard cell libraries are invaluable resources to design complex digital IC modules. The ASCEND-TSMC180-NCL library is a new contribution enabling better and faster design space exploration for asynchronous digital circuits design. It is intended to further the capability to design manufacturable ICs containing asynchronous modules.

This work was instrumental in putting to practice many if the subjects studied in the Author´s undergraduate course. Knowledge acquired in the courses of Microelectronics, Analog Electronics, Integrated Systems Design and Digital Circuits were used extensively. In addition to the knowledge from courses, contributed to this work non-curricular activities such as an undergraduate scholarship the Author was granted to develop hardware design within the scope of a project in cooperation with industrial partners.

Developing circuit to validate ASCEND-TSMC180-NCL library was essential to ensure that the proposed library could be used in conjunction with commercial EDA tools. The ASCEND-TSMC180-NCL library is fully compatible with the cells of the SAGE-X ARM commercial library, achieving the objective established for this work. To ensure manufacturability for the cells in ASCEND-TSMC180-NCL, a project is under way to develop modules using the library, and the module will be part of a mixed synchronous-asynchronous system on chip. The ASCEND-TSMC180-NCL library has been characterized in three corners (Slow, Normal and Fast).

Several possibilities for future work exist.

First, the Author suggests the implementation of smaller drive strength cells for all cell types in the library, to enable a better observation of the speed/power/area behavior of the library.

Extending the amount of cell types in the library is another obvious future work. For example, the literature pledges the use of 27 NCL gate types, deemed sufficient to efficiently implement any circuit in NCL [Fan05]. A study on how these 27 gates map to the other three gate classes used in SDDS-NCL circuits (INCL, NCLP and INCLP) is a future work that can determine the ideal composition for the library.

Also, maybe the most interesting application domain for QDI asynchronous circuits is low power circuits. Several works can be undertaken in this direction. One is evaluating the behavior of ASCEND-TSMC180-NCL cells under near- or subthreshold regimes. Another is designing cells specific for these regimes. These can support other QDI templates, more adequate to low power applications, such as the VELO template [Gua17].

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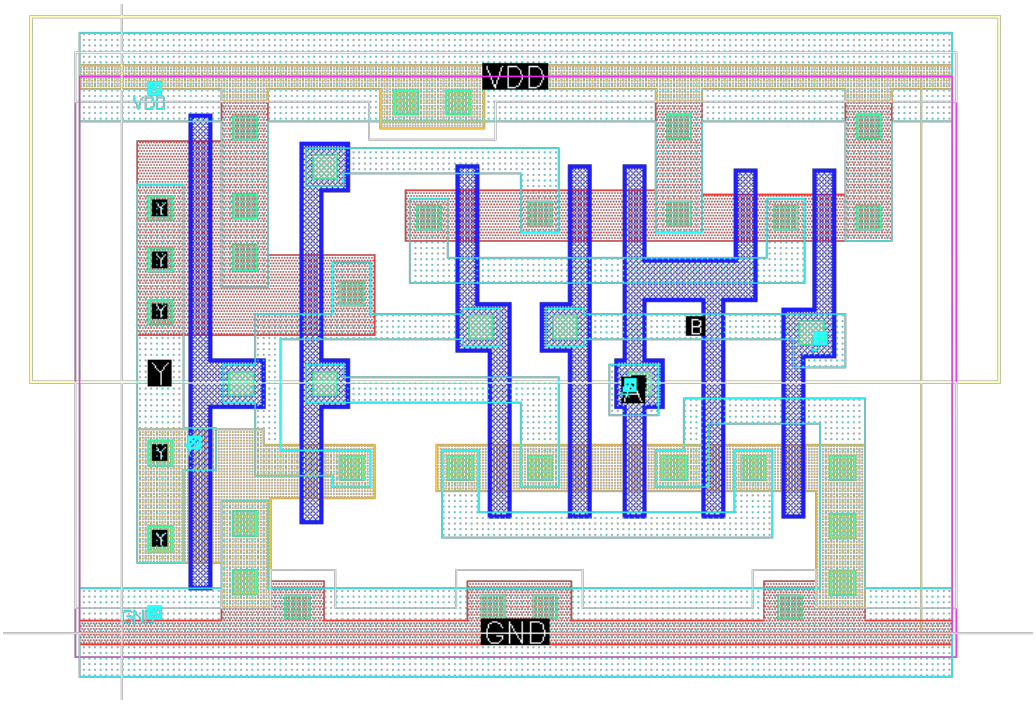
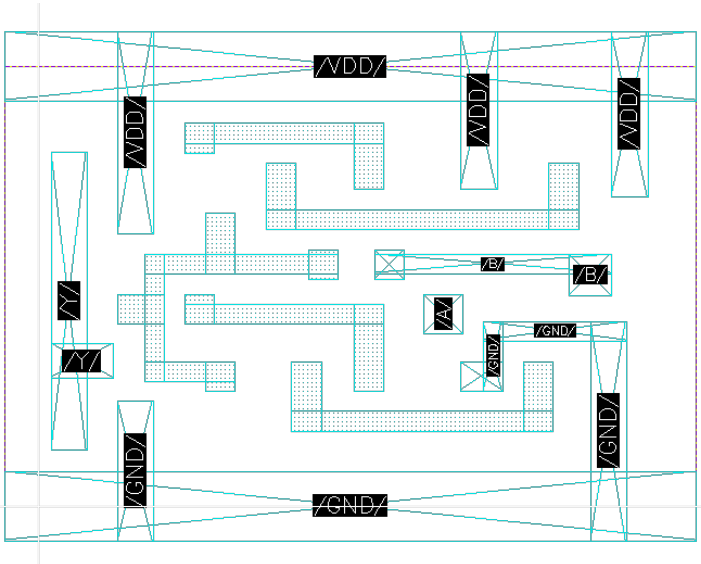
APPENDIX A – EXAMPLE CELL LAYOUT

Layout view for the INCL2W11OF2X2 cell.



Abstract view for the INCL2W11OF2X2 cell.



APPENDIX B – AN ASCEND-TSMC180-NCL LIBRARY DATASHEET (DATA CORRESPOND TO CHARACTERIZATION RESULTS FOR THE NOMINAL SUPPLY, 1.8V, AND TEMPERATURE OF 25ºC)

Below is a list of all 26 developed cells that compose the library. The 24 cells are divided into four groups according to the protocol (RTZ/RTO) they support, and according to the output inversion or not of their output. Following the same rules as the ARM compatible library, there are 4 possible cell drives available: XL, X1, X2 and X4. Not every drive is available for every cell type. There are 6 NCL cell types (corresponding to 9 cells), 2 inverted NCL cell types (corresponding to 5 cells), 4 NCLP cell types (corresponding to 7 cells) and 2 INCLP types (corresponding to 5 cells).

Cell Type	Drive Strength	Cell Function Description
NCL2W11OF2	XL X1 X2 X4	2-input NCL C-elements
NCL3W111OF3	X4	3-input NCL C-element
NCL2W211OF3	X4	3-input, threshold 2 NCL gate with 1 weight-2 input
NCL3W211OF3	X4	3-input, threshold 3 NCL gate with 1 weight-2 input
RNCL2W11OF2	X4	2-input NCL C-element with Reset
SNCL2W11OF2	X4	2-input NCL C-element with Set
INCL2W11OF2	XL X1 X2 X4	2-input NCL C-elements with inverted output
INCL3W111OF3	X4	3-input NCL C-element with inverted output
NCLP2W11OF2	XL X1 X2 X4	2-input NCLP C-elements
NCLP3W111OF3	X4	3-input NCLP C-element
NCL2W211OF3	X4	3-input, threshold 2, NCLP gate with 1 weight-2 input
NCLP3W211OF3	X4	3-input, threshold 3, NCLP gate with 1 weight-2 input
INCLP2W11OF2	XL X1 X2 X4	2-input, NCLP C-elements with inverted output
INCLP3W111OF3	X4	3-input, NCLP C-element with inverted output

The following pages in this Appendix correspond to a complete datasheet instance for the ASCEnD-TSMC180-NCL library. This is the Typical-Typical characterization datasheet, which corresponds to the expected responses of cells when operating under a 1.8V supply (the nominal suply voltage for the employed technology) at a temperature of 25ºC. Is is relevant to point out that the datasheet is automatically generated by the Cadence Liberate environment. Accordingly, the truth table for each cell is the virtual function, not the characteristic function. See Section 4.1 and Table 4.2 for more details on this subject.

NCL2W11OF2XL

ASCEND_TSMC180_NCL_TT_1.80V_25C Cell Library: Process , Voltage 1.80, Temp 25.00

Truth Table

INPUT		OUTPUT
A	B	Y
0	x	0
1	0	0
1	1	1

Footprint

Cell Name	Area
NCL2W11OF2XL	39.9168

Pin Capacitance Information

Cell Name	Pin Cap(pf)		Max Cap(pf)
	A	B	Y
NCL2W11OF2XL	0.00364	0.00432	0.11865

Leakage Information

Cell Name	Leakage(nW)		
	Min.	Avg	Max.
NCL2W11OF2XL	0.02081	0.03973	0.04518

Delay Information

Delay(ns) to Y rising (conditional):

Cell Name	Timing Arc(Dir)	When	Delay(ns)		
			Min	Mid	Max
NCL2W11OF2XL	A->Y (RR)	B	0.09222	0.16574	0.76116
	B->Y (RR)	A	0.09483	0.18423	0.83497

Delay(ns) to Y falling (conditional):

Cell Name	Timing Arc(Dir)	When	Delay(ns)		
			Min	Mid	Max
NCL2W11OF2XL	A->Y (FF)	!B	0.21291	0.31258	1.16983
	B->Y (FF)	!A	0.21785	0.33905	1.31930

Power Information

Internal switching power(pJ) to Y rising (conditional):

Cell Name	Input	When	Power(pJ)		
			min	mid	max

NCL2W11OF2XL	**A**	**B**	0.01057	0.01107	0.02097
	B	**A**	0.01137	0.01203	0.02231

Internal switching power(pJ) to Y falling (conditional):

Cell Name	**Input**	**When**	**Power(pJ)**		
			min	**mid**	**max**
NCL2W11OF2XL	**A**	**!B**	0.02006	0.01971	0.03169
	B	**!A**	0.01999	0.01957	0.03066

Passive power(pJ) for A rising (conditional):

Cell Name	**When**	**Power(pJ)**		
		min	**mid**	**max**
NCL2W11OF2XL	**B * Y**	-0.00213	-0.00231	-0.00236
	!B * !Y	-0.00239	-0.00239	-0.00240

Passive power(pJ) for A falling (conditional):

Cell Name	**When**	**Power(pJ)**		
		min	**mid**	**max**
NCL2W11OF2XL	**B * Y**	0.00260	0.00260	0.00261
	!B * !Y	0.00249	0.00244	0.00242

Passive power(pJ) for B rising (conditional):

Cell Name	**When**	**Power(pJ)**		
		min	**mid**	**max**
NCL2W11OF2XL	**A * Y**	-0.00145	-0.00151	-0.00154
	!A * !Y	-0.00202	-0.00203	-0.00203

Passive power(pJ) for B falling (conditional):

Cell Name	**When**	**Power(pJ)**		
		min	**mid**	**max**
NCL2W11OF2XL	**A * Y**	0.00191	0.00191	0.00191
	!A * !Y	0.00278	0.00275	0.00277

NCL2W11OF2X1

ASCEND_TSMC180_NCL_TT_1.80V_25C Cell Library: Process , Voltage 1.80, Temp 25.00

Truth Table

INPUT		OUTPUT
A	B	Y
0	x	0
1	0	0
1	1	1

Footprint

Cell Name	Area
NCL2W11OF2X1	43.2432

Pin Capacitance Information

Cell Name	Pin Cap(pf)		Max Cap(pf)
	A	B	Y
NCL2W11OF2X1	0.00448	0.00444	0.11865

Leakage Information

Cell Name	Leakage(nW)		
	Min.	Avg	Max.
NCL2W11OF2X1	0.02446	0.04206	0.04882

Delay Information

Delay(ns) to Y rising (conditional):

Cell Name	Timing Arc(Dir)	When	Delay(ns)		
			Min	Mid	Max
NCL2W11OF2X1	A->Y (RR)	B	0.10362	0.16854	0.57064
	B->Y (RR)	A	0.10354	0.18651	0.64527

Delay(ns) to Y falling (conditional):

Cell Name	Timing Arc(Dir)	When	Delay(ns)		
			Min	Mid	Max
NCL2W11OF2X1	A->Y (FF)	!B	0.23445	0.32257	1.08440
	B->Y (FF)	!A	0.23261	0.34423	1.23498

Power Information

Internal switching power(pJ) to Y rising (conditional):

Cell Name	Input	When	Power(pJ)		
			min	mid	max

NCL2W11OF2X1	**A**	**B**	0.01257	0.01299	0.02300
	B	**A**	0.01338	0.01416	0.02469

Internal switching power(pJ) to Y falling (conditional):

Cell Name	**Input**	**When**	**Power(pJ)**		
			min	**mid**	**max**
NCL2W11OF2X1	**A**	**!B**	0.02382	0.02301	0.03522
	B	**!A**	0.02346	0.02268	0.03419

Passive power(pJ) for A rising (conditional):

Cell Name	**When**	**Power(pJ)**		
		min	**mid**	**max**
NCL2W11OF2X1	**B * Y**	-0.00232	-0.00251	-0.00256
	!B * !Y	-0.00279	-0.00280	-0.00279

Passive power(pJ) for A falling (conditional):

Cell Name	**When**	**Power(pJ)**		
		min	**mid**	**max**
NCL2W11OF2X1	**B * Y**	0.00279	0.00281	0.00280
	!B * !Y	0.00289	0.00283	0.00284

Passive power(pJ) for B rising (conditional):

Cell Name	**When**	**Power(pJ)**		
		min	**mid**	**max**
NCL2W11OF2X1	**A * Y**	-0.00162	-0.00170	-0.00173
	!A * !Y	-0.00201	-0.00201	-0.00202

Passive power(pJ) for B falling (conditional):

Cell Name	**When**	**Power(pJ)**		
		min	**mid**	**max**
NCL2W11OF2X1	**A * Y**	0.00216	0.00217	0.00217
	!A * !Y	0.00279	0.00274	0.00276

NCL2W11OF2X2

ASCEND_TSMC180_NCL_TT_1.80V_25C Cell Library: Process , Voltage 1.80, Temp 25.00

Truth Table

INPUT		OUTPUT
A	B	Y
0	x	0
1	0	0
1	1	1

Footprint

Cell Name	Area
NCL2W11OF2X2	36.5904

Pin Capacitance Information

Cell Name	Pin Cap(pf)		Max Cap(pf)
	A	B	Y
NCL2W11OF2X2	0.00365	0.00417	0.11865

Leakage Information

Cell Name	Leakage(nW)		
	Min.	Avg	Max.
NCL2W11OF2X2	0.02996	0.04846	0.05433

Delay Information

Delay(ns) to Y rising (conditional):

Cell Name	Timing Arc(Dir)	When	Delay(ns)		
			Min	Mid	Max
NCL2W11OF2X2	A->Y (RR)	B	0.10565	0.15786	0.33738
	B->Y (RR)	A	0.10759	0.17802	0.41536

Delay(ns) to Y falling (conditional):

Cell Name	Timing Arc(Dir)	When	Delay(ns)		
			Min	Mid	Max
NCL2W11OF2X2	A->Y (FF)	!B	0.27165	0.34514	0.99590
	B->Y (FF)	!A	0.27692	0.37113	1.15487

Power Information

Internal switching power(pJ) to Y rising (conditional):

Cell Name	Input	When	Power(pJ)		
			min	mid	max

NCL2W11OF2X2	**A**	**B**	0.01584	0.01648	0.02766
	B	**A**	0.01665	0.01771	0.02937

Internal switching power(pJ) to Y falling (conditional):

Cell Name	**Input**	**When**	**Power(pJ)**		
			min	**mid**	**max**
NCL2W11OF2X2	**A**	**!B**	0.03108	0.02935	0.03882
	B	**!A**	0.03105	0.02912	0.03819

Passive power(pJ) for A rising (conditional):

Cell Name	**When**	**Power(pJ)**		
		min	**mid**	**max**
NCL2W11OF2X2	**B * Y**	-0.00206	-0.00222	-0.00227
	!B * !Y	-0.00237	-0.00237	-0.00238

Passive power(pJ) for A falling (conditional):

Cell Name	**When**	**Power(pJ)**		
		min	**mid**	**max**
NCL2W11OF2X2	**B * Y**	0.00250	0.00250	0.00249
	!B * !Y	0.00248	0.00241	0.00240

Passive power(pJ) for B rising (conditional):

Cell Name	**When**	**Power(pJ)**		
		min	**mid**	**max**
NCL2W11OF2X2	**A * Y**	-0.00140	-0.00147	-0.00148
	!A * !Y	-0.00194	-0.00194	-0.00194

Passive power(pJ) for B falling (conditional):

Cell Name	**When**	**Power(pJ)**		
		min	**mid**	**max**
NCL2W11OF2X2	**A * Y**	0.00181	0.00181	0.00182
	!A * !Y	0.00261	0.00256	0.00257

NCL2W11OF2X4

ASCEND_TSMC180_NCL_TT_1.80V_25C Cell Library: Process , Voltage 1.80, Temp 25.00

Truth Table

INPUT		OUTPUT
A	B	Y
0	x	0
1	0	0
1	1	1

Footprint

Cell Name	Area
NCL2W11OF2X4	43.2432

Pin Capacitance Information

Cell Name	Pin Cap(pf)		Max Cap(pf)
	A	B	Y
NCL2W11OF2X4	0.00409	0.00432	0.11865

Leakage Information

Cell Name	Leakage(nW)		
	Min.	Avg	Max.
NCL2W11OF2X4	0.05084	0.07583	0.08634

Delay Information

Delay(ns) to Y rising (conditional):

Cell Name	Timing Arc(Dir)	When	Delay(ns)		
			Min	Mid	Max
NCL2W11OF2X4	A->Y (RR)	B	0.15384	0.20545	0.33989
	B->Y (RR)	A	0.15700	0.22886	0.43400

Delay(ns) to Y falling (conditional):

Cell Name	Timing Arc(Dir)	When	Delay(ns)		
			Min	Mid	Max
NCL2W11OF2X4	A->Y (FF)	!B	0.32122	0.38597	0.96077
	B->Y (FF)	!A	0.32495	0.41092	1.14250

Power Information

Internal switching power(pJ) to Y rising (conditional):

Cell Name	Input	When	Power(pJ)		
			min	mid	max

NCL2W11OF2X4	**A**	**B**	0.03547	0.03499	0.05371
	B	**A**	0.03651	0.03649	0.05727

Internal switching power(pJ) to Y falling (conditional):

Cell Name	**Input**	**When**	**Power(pJ)**		
			min	**mid**	**max**
NCL2W11OF2X4	**A**	**!B**	0.06747	0.06369	0.07056
	B	**!A**	0.06710	0.06328	0.07349

Passive power(pJ) for A rising (conditional):

Cell Name	**When**	**Power(pJ)**		
		min	**mid**	**max**
NCL2W11OF2X4	**B * Y**	-0.00245	-0.00268	-0.00277
	!B * !Y	-0.00283	-0.00284	-0.00284

Passive power(pJ) for A falling (conditional):

Cell Name	**When**	**Power(pJ)**		
		min	**mid**	**max**
NCL2W11OF2X4	**B * Y**	0.00308	0.00308	0.00309
	!B * !Y	0.00294	0.00287	0.00287

Passive power(pJ) for B rising (conditional):

Cell Name	**When**	**Power(pJ)**		
		min	**mid**	**max**
NCL2W11OF2X4	**A * Y**	-0.00150	-0.00157	-0.00161
	!A * !Y	-0.00227	-0.00228	-0.00228

Passive power(pJ) for B falling (conditional):

Cell Name	**When**	**Power(pJ)**		
		min	**mid**	**max**
NCL2W11OF2X4	**A * Y**	0.00208	0.00209	0.00209
	!A * !Y	0.00304	0.00301	0.00302

NCL3W111OF3X4

ASCEND_TSMC180_NCL_TT_1.80V_25C Cell Library: Process , Voltage 1.80, Temp 25.00

Truth Table

INPUT			OUTPUT
A	B	C	Y
0	x	x	0
1	0	x	0
1	1	0	0
1	1	1	1

Footprint

Cell Name	Area
NCL3W111OF3X4	49.8960

Pin Capacitance Information

Cell Name	Pin Cap(pf)			Max Cap(pf)
	A	B	C	Y
NCL3W111OF3X4	0.00705	0.00688	0.00709	0.11865

Leakage Information

Cell Name	Leakage(nW)		
	Min.	Avg	Max.
NCL3W111OF3X4	0.04441	0.07204	0.08690

Delay Information

Delay(ns) to Y rising (conditional):

Cell Name	Timing Arc(Dir)	When	Delay(ns)		
			Min	Mid	Max
NCL3W111OF3X4	A->Y (RR)	B * C	0.11228	0.14139	0.10418
	B->Y (RR)	A * C	0.10957	0.15309	0.16146
	C->Y (RR)	A * B	0.10799	0.16759	0.21112

Delay(ns) to Y falling (conditional):

Cell Name	Timing Arc(Dir)	When	Delay(ns)		
			Min	Mid	Max
NCL3W111OF3X4	A->Y (FF)	!B * !C	0.26710	0.31068	0.67015
	B->Y (FF)	!A * !C	0.26390	0.32332	0.81961
	C->Y (FF)	!A * !B	0.24830	0.32325	0.92070

Power Information

Internal switching power(pJ) to Y rising (conditional):

Cell Name	Input	When	Power(pJ)		
			min	mid	max
NCL3W111OF3X4	A	B * C	0.02594	0.02618	0.04145
	B	A * C	0.02726	0.02850	0.04489
	C	A * B	0.02814	0.02957	0.04641

Internal switching power(pJ) to Y falling (conditional):

Cell Name	Input	When	Power(pJ)		
			min	mid	max
NCL3W111OF3X4	A	!B * !C	0.05792	0.05528	0.06828
	B	!A * !C	0.05621	0.05415	0.06737
	C	!A * !B	0.05454	0.05215	0.06754

Passive power(pJ) for A rising (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
NCL3W111OF3X4	B * C * Y	-0.00430	-0.00446	-0.00456
	B * !C * Y	-0.00475	-0.00476	-0.00477
	B * !C * !Y	-0.00475	-0.00478	-0.00476
	!B * C * Y	-0.00444	-0.00465	-0.00477
	!B * C * !Y	-0.00442	-0.00462	-0.00471
	!B * !C * !Y	-0.00490	-0.00492	-0.00492

Passive power(pJ) for A falling (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
NCL3W111OF3X4	B * C * Y	0.00472	0.00475	0.00476
	B * !C * Y	0.00476	0.00476	0.00477
	B * !C * !Y	0.00480	0.00480	0.00476
	!B * C * Y	0.00624	0.00627	0.00628
	!B * C * !Y	0.00478	0.00471	0.00471
	!B * !C * !Y	0.00495	0.00494	0.00492

Passive power(pJ) for B rising (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
NCL3W111OF3X4	A * C * Y	-0.00269	-0.00277	-0.00279
	A * !C * Y	-0.00322	-0.00325	-0.00324
	A * !C * !Y	-0.00417	-0.00418	-0.00416
	!A * C * Y	-0.00319	-0.00321	-0.00327
	!A * C * !Y	-0.00316	-0.00319	-0.00324
	!A * !C * !Y	-0.00433	-0.00434	-0.00434

Passive power(pJ) for B falling (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
NCL3W111OF3X4	A * C * Y	0.00286	0.00287	0.00288
	A * !C * Y	0.00322	0.00325	0.00324
	A * !C * !Y	0.00430	0.00419	0.00416
	!A * C * Y	0.00443	0.00443	0.00445
	!A * C * !Y	0.00481	0.00485	0.00487
	!A * !C * !Y	0.00437	0.00435	0.00435

Passive power(pJ) for C rising (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
NCL3W111OF3X4	A * B * Y	-0.00194	-0.00201	-0.00203
	A * !B * Y	-0.00291	-0.00307	-0.00325
	A * !B * !Y	-0.00291	-0.00307	-0.00326
	!A * B * Y	-0.00232	-0.00233	-0.00238
	!A * B * !Y	-0.00232	-0.00233	-0.00238
	!A * !B * !Y	-0.00338	-0.00338	-0.00340

Passive power(pJ) for C falling (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
NCL3W111OF3X4	A * B * Y	0.00298	0.00297	0.00297
	A * !B * Y	0.00325	0.00327	0.00325
	A * !B * !Y	0.00453	0.00452	0.00453
	!A * B * Y	0.00291	0.00294	0.00292
	!A * B * !Y	0.00465	0.00466	0.00466
	!A * !B * !Y	0.00489	0.00485	0.00486

NCL2W211OF3X4

ASCEND_TSMC180_NCL_TT_1.80V_25C Cell Library: Process , Voltage 1.80, Temp 25.00

Truth Table

INPUT			OUTPUT
A	B	C	Y
0	0	x	0
0	1	0	0
x	1	1	1
1	x	x	1

Footprint

Cell Name	Area
NCL2W211OF3X4	49.8960

Pin Capacitance Information

Cell Name	Pin Cap(pf)			Max Cap(pf)
	A	B	C	Y
NCL2W211OF3X4	0.00695	0.00655	0.00659	0.11865

Leakage Information

Cell Name	Leakage(nW)		
	Min.	Avg	Max.
NCL2W211OF3X4	0.06745	0.08267	0.09070

Delay Information

Delay(ns) to Y rising (conditional):

Cell Name	Timing Arc(Dir)	When	Delay(ns)		
			Min	Mid	Max
NCL2W211OF3X4	A->Y (RR)	B * !C	0.09458	0.16060	0.20688
	A->Y (RR)	!B * C	0.08718	0.14935	0.17460
	A->Y (RR)	!B * !C	0.10407	0.17732	0.45727
	B->Y (RR)	!A * C	0.12477	0.17260	0.22758
	C->Y (RR)	!A * B	0.12986	0.19967	0.31803

Delay(ns) to Y falling (conditional):

Cell Name	Timing Arc(Dir)	When	Delay(ns)		
			Min	Mid	Max
NCL2W211OF3X4	A->Y (FF)	!B * !C	0.26183	0.30706	0.82394
	B->Y (FF)	!A * !C	0.24093	0.30010	0.78397
	C->Y (FF)	!A * !B	0.22467	0.30174	0.88417

Power Information

Internal switching power(pJ) to Y rising (conditional):

Cell Name	Input	When	Power(pJ)		
			min	mid	max
NCL2W211OF3X4	A	B * !C	0.02625	0.02826	0.04341
	A	!B * C	0.02446	0.02686	0.04295
	A	!B * !C	0.02952	0.03189	0.06979
	B	!A * C	0.02791	0.02807	0.04375
	C	!A * B	0.03012	0.03108	0.04760

Internal switching power(pJ) to Y falling (conditional):

Cell Name	Input	When	Power(pJ)		
			min	mid	max
NCL2W211OF3X4	A	!B * !C	0.05877	0.05641	0.08431
	B	!A * !C	0.05553	0.05365	0.06948
	C	!A * !B	0.05375	0.05194	0.06974

Passive power(pJ) for A rising (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
NCL2W211OF3X4	B * C * Y	-0.00412	-0.00424	-0.00431
	B * !C * Y	-0.00411	-0.00447	-0.00451
	!B * C * Y	-0.00410	-0.00446	-0.00454

Passive power(pJ) for A falling (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
NCL2W211OF3X4	B * C * Y	0.00430	0.00432	0.00434
	B * !C * Y	0.00481	0.00485	0.00484
	!B * C * Y	0.00496	0.00499	0.00497

Passive power(pJ) for B rising (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
NCL2W211OF3X4	A * C * Y	-0.00299	-0.00305	-0.00305
	A * !C * Y	-0.00242	-0.00244	-0.00244
	!A * C * Y	-0.00397	-0.00447	-0.00463
	!A * !C * !Y	-0.00493	-0.00495	-0.00495

Passive power(pJ) for B falling (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
	A * C * Y	0.00325	0.00326	0.00327

NCL2W211OF3X4	**A * !C * Y**	0.00350	0.00347	0.00348
	!A * C * Y	0.00492	0.00496	0.00495
	!A * !C * !Y	0.00505	0.00498	0.00500

Passive power(pJ) for C rising (conditional):

Cell Name	**When**	**Power(pJ)**		
		min	**mid**	**max**
NCL2W211OF3X4	**A * B * Y**	-0.00199	-0.00204	-0.00206
	A * !B * Y	-0.00205	-0.00207	-0.00206
	!A * B * Y	-0.00199	-0.00206	-0.00210
	!A * !B * !Y	-0.00386	-0.00388	-0.00388

Passive power(pJ) for C falling (conditional):

Cell Name	**When**	**Power(pJ)**		
		min	**mid**	**max**
NCL2W211OF3X4	**A * B * Y**	0.00313	0.00315	0.00313
	A * !B * Y	0.00539	0.00542	0.00543
	!A * B * Y	0.00350	0.00350	0.00350
	!A * !B * !Y	0.00492	0.00490	0.00493

NCL3W211OF3X4

ASCEND_TSMC180_NCL_TT_1.80V_25C Cell Library: Process , Voltage 1.80, Temp 25.00

Truth Table

INPUT			OUTPUT
A	B	C	Y
0	x	x	0
1	0	0	0
1	x	1	1
1	1	x	1

Footprint

Cell Name	Area
NCL3W211OF3X4	49.8960

Pin Capacitance Information

Cell Name	Pin Cap(pf)			Max Cap(pf)
	A	B	C	Y
NCL3W211OF3X4	0.00618	0.00603	0.00607	0.11865

Leakage Information

Cell Name	Leakage(nW)		
	Min.	Avg	Max.
NCL3W211OF3X4	0.04965	0.07652	0.08577

Delay Information

Delay(ns) to Y rising (conditional):

Cell Name	Timing Arc(Dir)	When	Delay(ns)		
			Min	Mid	Max
NCL3W211OF3X4	A->Y (RR)	B * C	0.10372	0.17127	0.26169
	A->Y (RR)	B * !C	0.12612	0.19499	0.32612
	A->Y (RR)	!B * C	0.12242	0.19237	0.32886
	B->Y (RR)	A * !C	0.12452	0.17264	0.22604
	C->Y (RR)	A * !B	0.12440	0.17143	0.20408

Delay(ns) to Y falling (conditional):

Cell Name	Timing Arc(Dir)	When	Delay(ns)		
			Min	Mid	Max
NCL3W211OF3X4	A->Y (FF)	!B * !C	0.25496	0.33394	0.96476
	B->Y (FF)	!A * !C	0.27271	0.33263	0.85944
	C->Y (FF)	!A * !B	0.28285	0.32711	0.71391

Power Information

Internal switching power(pJ) to Y rising (conditional):

Cell Name	Input	When	Power(pJ)		
			min	mid	max
NCL3W211OF3X4	A	B * C	0.02758	0.02939	0.04611
	A	B * !C	0.02986	0.03081	0.04769
	A	!B * C	0.02906	0.03043	0.04675
	B	A * !C	0.02809	0.02833	0.04407
	C	A * !B	0.02755	0.02785	0.04147

Internal switching power(pJ) to Y falling (conditional):

Cell Name	Input	When	Power(pJ)		
			min	mid	max
NCL3W211OF3X4	A	!B * !C	0.05414	0.05188	0.06564
	B	!A * !C	0.05533	0.05285	0.06486
	C	!A * !B	0.05763	0.05475	0.06638

Passive power(pJ) for A rising (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
NCL3W211OF3X4	B * C * Y	-0.00195	-0.00206	-0.00209
	B * !C * Y	-0.00193	-0.00203	-0.00208
	!B * C * Y	-0.00191	-0.00202	-0.00204
	!B * !C * !Y	-0.00215	-0.00215	-0.00216

Passive power(pJ) for A falling (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
NCL3W211OF3X4	B * C * Y	0.00301	0.00302	0.00302
	B * !C * Y	0.00329	0.00330	0.00330
	!B * C * Y	0.00480	0.00482	0.00482
	!B * !C * !Y	0.00446	0.00444	0.00442

Passive power(pJ) for B rising (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
NCL3W211OF3X4	A * C * Y	-0.00259	-0.00262	-0.00263
	A * !C * Y	-0.00337	-0.00379	-0.00392
	!A * C * Y	-0.00186	-0.00188	-0.00190
	!A * C * !Y	-0.00390	-0.00391	-0.00392
	!A * !C * !Y	-0.00411	-0.00412	-0.00412

Passive power(pJ) for B falling (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
NCL3W211OF3X4	A * C * Y	0.00274	0.00273	0.00275
	A * !C * Y	0.00422	0.00425	0.00424
	!A * C * Y	0.00316	0.00316	0.00316
	!A * C * !Y	0.00390	0.00391	0.00392
	!A * !C * !Y	0.00423	0.00415	0.00418

Passive power(pJ) for C rising (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
NCL3W211OF3X4	A * B * Y	-0.00362	-0.00370	-0.00374
	A * !B * Y	-0.00361	-0.00398	-0.00405
	!A * B * Y	-0.00380	-0.00401	-0.00408
	!A * B * !Y	-0.00428	-0.00430	-0.00433
	!A * !B * !Y	-0.00450	-0.00449	-0.00452

Passive power(pJ) for C falling (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
NCL3W211OF3X4	A * B * Y	0.00377	0.00379	0.00380
	A * !B * Y	0.00456	0.00456	0.00459
	!A * B * Y	0.00434	0.00436	0.00438
	!A * B * !Y	0.00428	0.00430	0.00433
	!A * !B * !Y	0.00461	0.00454	0.00458

RNCL2W11OF2X4

ASCEND_TSMC180_NCL_TT_1.80V_25C Cell Library: Process , Voltage 1.80, Temp 25.00

Truth Table

INPUT				OUTPUT
A	B	RN	G	Y
x	x	0	x	0
x	x	1	0	IQ
0	x	1	1	0
1	0	1	1	0
1	1	1	1	1

Footprint

Cell Name	Area
RNCL2W11OF2X4	49.8960

Pin Capacitance Information

Cell Name	Pin Cap(pf)				Max Cap(pf)
	A	B	RN	G	Y
RNCL2W11OF2X4	0.00624	0.00626	0.00658	0.00000	0.11865

Leakage Information

Cell Name	Leakage(nW)		
	Min.	Avg	Max.
RNCL2W11OF2X4	0.03736	0.06304	0.09364

Delay Information

Delay(ns) to Y rising (conditional):

Cell Name	Timing Arc(Dir)	When	Delay(ns)		
			Min	Mid	Max
RNCL2W11OF2X4	A->Y (RR)	B * RN	0.14639	0.19750	0.31118
	B->Y (RR)	A * RN	0.14987	0.21701	0.37904
	RN->Y (RR)	A * B	0.15754	0.19418	0.45660

Delay(ns) to Y falling (conditional):

Cell Name	Timing Arc(Dir)	When	Delay(ns)		
			Min	Mid	Max
RNCL2W11OF2X4	A->Y (FF)	!B * RN	0.20329	0.26086	0.66125
	B->Y (FF)	!A * RN	0.20101	0.28184	0.81948
	RN->Y (FF)	A * B	0.12170	0.21429	0.77805
	RN->Y (FF)	A * !B	0.10668	0.19080	0.55735
	RN->Y (FF)	!A * B	0.11330	0.19830	0.56652

Constraint Information

Min Pulse Width (ns) for RN:

Cell Name	High	Low
RNCL2W11OF2X4	-	3.0005

Power Information

Internal switching power(pJ) to Y rising (conditional):

Cell Name	Input	When	Power(pJ)		
			min	mid	max
RNCL2W11OF2X4	**A**	**B * RN**	0.03150	0.03158	0.04784
	B	**A * RN**	0.03338	0.03349	0.05044
	RN	**A * B**	0.03227	0.03211	0.06718

Internal switching power(pJ) to Y falling (conditional):

Cell Name	Input	When	Power(pJ)		
			min	mid	max
RNCL2W11OF2X4	**A**	**!B * RN**	0.05031	0.04888	0.06548
	B	**!A * RN**	0.04963	0.04825	0.06734
	RN	**A * B**	0.04405	0.04630	0.08408
	RN	**A * !B**	0.04070	0.04298	0.06620
	RN	**!A * B**	0.04098	0.04279	0.06551

Passive power(pJ) for A rising (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
RNCL2W11OF2X4	**B * RN * Y**	-0.00346	-0.00376	-0.00385
	B * !RN * !Y	-0.00344	-0.00348	-0.00351
	!B * RN * !Y	-0.00411	-0.00415	-0.00415
	!B * !RN * !Y	-0.00413	-0.00417	-0.00416

Passive power(pJ) for A falling (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
RNCL2W11OF2X4	**B * RN * Y**	0.00406	0.00408	0.00409
	B * !RN * !Y	0.00447	0.00447	0.00446
	!B * RN * !Y	0.00429	0.00418	0.00417
	!B * !RN * !Y	0.00487	0.00488	0.00495

Passive power(pJ) for B rising (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
	A * RN * Y	-0.00212	-0.00221	-0.00223

RNCL2W11OF2X4	**A * !RN * !Y**	-0.00106	-0.00106	-0.00112
	!A * RN * !Y	-0.00349	-0.00350	-0.00349
	!A * !RN * !Y	-0.00352	-0.00353	-0.00355

Passive power(pJ) for B falling (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
RNCL2W11OF2X4	**A * RN * Y**	0.00334	0.00335	0.00334
	A * !RN * !Y	0.00459	0.00460	0.00462
	!A * RN * !Y	0.00462	0.00459	0.00460
	!A * !RN * !Y	0.00459	0.00458	0.00463

Passive power(pJ) for RN rising (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
RNCL2W11OF2X4	**A * !B * !Y**	-0.00430	-0.00430	-0.00431
	!A * B * !Y	-0.00430	-0.00431	-0.00432
	!A * !B * !Y	-0.00430	-0.00431	-0.00433

Passive power(pJ) for RN falling (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
RNCL2W11OF2X4	**A * !B * !Y**	0.00442	0.00434	0.00434
	!A * B * !Y	0.00452	0.00440	0.00441
	!A * !B * !Y	0.00462	0.00463	0.00462

SNCL2W11OF2X4

ASCEND_TSMC180_NCL_TT_1.80V_25C Cell Library: Process , Voltage 1.80, Temp 25.00

Truth Table

INPUT				OUTPUT
A	B	S	G	Y
x	x	0	0	IQ
0	x	0	1	0
x	x	1	x	1
1	0	0	1	0
1	1	x	1	1

Footprint

Cell Name	Area
SNCL2W11OF2X4	49.8960

Pin Capacitance Information

Cell Name	Pin Cap(pf)				Max Cap(pf)
	A	B	S	G	Y
SNCL2W11OF2X4	0.00659	0.00659	0.00695	0.00000	0.11865

Leakage Information

Cell Name	Leakage(nW)		
	Min.	Avg	Max.
SNCL2W11OF2X4	0.06745	0.08267	0.09070

Delay Information

Delay(ns) to Y rising (conditional):

Cell Name	Timing Arc(Dir)	When	Delay(ns)		
			Min	Mid	Max
SNCL2W11OF2X4	A->Y (RR)	B * !S	0.12477	0.17260	0.22758
	B->Y (RR)	A * !S	0.12986	0.19967	0.31803
	S->Y (RR)	A * !B	0.09458	0.16060	0.20688
	S->Y (RR)	!A * B	0.08718	0.14935	0.17460
	S->Y (RR)	!A * !B	0.10407	0.17732	0.45727

Delay(ns) to Y falling (conditional):

Cell Name	Timing Arc(Dir)	When	Delay(ns)		
			Min	Mid	Max
SNCL2W11OF2X4	A->Y (FF)	!B * !S	0.24402	0.30293	0.78393
	B->Y (FF)	!A * !S	0.22467	0.30174	0.88417
	S->Y (FF)	!A * !B	0.26183	0.30706	0.82394

Constraint Information

Min Pulse Width (ns) for S:

Cell Name	High	Low
SNCL2W11OF2X4	3.0005	-

Power Information

Internal switching power(pJ) to Y rising (conditional):

Cell Name	Input	When	Power(pJ)		
			min	mid	max
SNCL2W11OF2X4	A	B * !S	0.02791	0.02807	0.04375
	B	A * !S	0.03012	0.03108	0.04760
	S	A * !B	0.02625	0.02826	0.04341
	S	!A * B	0.02446	0.02686	0.04295
	S	!A * !B	0.02952	0.03189	0.06979

Internal switching power(pJ) to Y falling (conditional):

Cell Name	Input	When	Power(pJ)		
			min	mid	max
SNCL2W11OF2X4	A	!B * !S	0.05575	0.05377	0.06929
	B	!A * !S	0.05375	0.05194	0.06974
	S	!A * !B	0.05877	0.05641	0.08431

Passive power(pJ) for A rising (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
SNCL2W11OF2X4	B * S * Y	-0.00299	-0.00305	-0.00305
	B * !S * Y	-0.00397	-0.00447	-0.00463
	!B * S * Y	-0.00242	-0.00244	-0.00244
	!B * !S * !Y	-0.00493	-0.00495	-0.00495

Passive power(pJ) for A falling (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
SNCL2W11OF2X4	B * S * Y	0.00325	0.00326	0.00327
	B * !S * Y	0.00492	0.00496	0.00495
	!B * S * Y	0.00350	0.00347	0.00348
	!B * !S * !Y	0.00505	0.00498	0.00500

Passive power(pJ) for B rising (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
	A * S * Y	-0.00199	-0.00204	-0.00206

SNCL2W11OF2X4	**A * !S * Y**	-0.00196	-0.00203	-0.00206
	!A * S * Y	-0.00205	-0.00207	-0.00206
	!A * !S * !Y	-0.00386	-0.00388	-0.00388

Passive power(pJ) for B falling (conditional):

Cell Name	**When**	**Power(pJ)**		
		min	**mid**	**max**
SNCL2W11OF2X4	**A * S * Y**	0.00313	0.00315	0.00313
	A * !S * Y	0.00350	0.00350	0.00350
	!A * S * Y	0.00539	0.00542	0.00543
	!A * !S * !Y	0.00492	0.00490	0.00493

Passive power(pJ) for S rising (conditional):

Cell Name	**When**	**Power(pJ)**		
		min	**mid**	**max**
SNCL2W11OF2X4	**A * B * Y**	-0.00412	-0.00424	-0.00431
	A * !B * Y	-0.00431	-0.00457	-0.00460
	!A * B * Y	-0.00410	-0.00446	-0.00454

Passive power(pJ) for S falling (conditional):

Cell Name	**When**	**Power(pJ)**		
		min	**mid**	**max**
SNCL2W11OF2X4	**A * B * Y**	0.00430	0.00432	0.00434
	A * !B * Y	0.00481	0.00485	0.00484
	!A * B * Y	0.00496	0.00499	0.00497

INCL2W11OF2XL

ASCEND_TSMC180_NCL_TT_1.80V_25C Cell Library: Process , Voltage 1.80, Temp 25.00

Truth Table

INPUT		OUTPUT
A	B	Y
0	x	1
1	0	1
1	1	0

Footprint

Cell Name	Area
INCL2W11OF2XL	39.9168

Pin Capacitance Information

Cell Name	Pin Cap(pf)		Max Cap(pf)
	A	B	Y
INCL2W11OF2XL	0.00352	0.00414	0.11865

Leakage Information

Cell Name	Leakage(nW)		
	Min.	Avg	Max.
INCL2W11OF2XL	0.02529	0.03970	0.06143

Delay Information

Delay(ns) to Y rising (conditional):

Cell Name	Timing Arc(Dir)	When	Delay(ns)		
			Min	Mid	Max
INCL2W11OF2XL	A->Y (FR)	!B	0.22777	0.31867	1.44950
	B->Y (FR)	!A	0.23060	0.34585	1.58760

Delay(ns) to Y falling (conditional):

Cell Name	Timing Arc(Dir)	When	Delay(ns)		
			Min	Mid	Max
INCL2W11OF2XL	A->Y (RF)	B	0.14945	0.20328	0.46920
	B->Y (RF)	A	0.15164	0.21828	0.53427

Power Information

Internal switching power(pJ) to Y rising (conditional):

Cell Name	Input	When	Power(pJ)		
			min	mid	max

INCL2W11OF2XL	**A**	**!B**	0.01726	0.01764	0.03046
	B	**!A**	0.01710	0.01753	0.02915

Internal switching power(pJ) to Y falling (conditional):

Cell Name	**Input**	**When**	**Power(pJ)**		
			min	**mid**	**max**
INCL2W11OF2XL	**A**	**B**	0.01085	0.01116	0.02008
	B	**A**	0.01164	0.01196	0.02119

Passive power(pJ) for A rising (conditional):

Cell Name	**When**	**Power(pJ)**		
		min	**mid**	**max**
INCL2W11OF2XL	**B * !Y**	-0.00208	-0.00225	-0.00230
	!B * Y	-0.00234	-0.00234	-0.00235

Passive power(pJ) for A falling (conditional):

Cell Name	**When**	**Power(pJ)**		
		min	**mid**	**max**
INCL2W11OF2XL	**B * !Y**	0.00254	0.00254	0.00254
	!B * Y	0.00244	0.00239	0.00237

Passive power(pJ) for B rising (conditional):

Cell Name	**When**	**Power(pJ)**		
		min	**mid**	**max**
INCL2W11OF2XL	**A * !Y**	-0.00141	-0.00148	-0.00149
	!A * Y	-0.00193	-0.00192	-0.00193

Passive power(pJ) for B falling (conditional):

Cell Name	**When**	**Power(pJ)**		
		min	**mid**	**max**
INCL2W11OF2XL	**A * !Y**	0.00184	0.00185	0.00186
	!A * Y	0.00270	0.00265	0.00266

INCL2W11OF2X1

ASCEND_TSMC180_NCL_TT_1.80V_25C Cell Library: Process , Voltage 1.80, Temp 25.00

Truth Table

INPUT		OUTPUT
A	B	Y
0	x	1
1	0	1
1	1	0

Footprint

Cell Name	Area
INCL2W11OF2X1	43.2432

Pin Capacitance Information

Cell Name	Pin Cap(pf)		Max Cap(pf)
	A	B	Y
INCL2W11OF2X1	0.00453	0.00444	0.11865

Leakage Information

Cell Name	Leakage(nW)		
	Min.	Avg	Max.
INCL2W11OF2X1	0.02763	0.04206	0.06376

Delay Information

Delay(ns) to Y rising (conditional):

Cell Name	Timing Arc(Dir)	When	Delay(ns)		
			Min	Mid	Max
INCL2W11OF2X1	A->Y (FR)	!B	0.25205	0.33116	1.26079
	B->Y (FR)	!A	0.24938	0.35372	1.40217

Delay(ns) to Y falling (conditional):

Cell Name	Timing Arc(Dir)	When	Delay(ns)		
			Min	Mid	Max
INCL2W11OF2X1	A->Y (RF)	B	0.14536	0.19300	0.36799
	B->Y (RF)	A	0.14519	0.20846	0.43703

Power Information

Internal switching power(pJ) to Y rising (conditional):

Cell Name	Input	When	Power(pJ)		
			min	mid	max

INCL2W11OF2X1	**A**	**!B**	0.02045	0.02071	0.03416
	B	**!A**	0.02006	0.02040	0.03276

Internal switching power(pJ) to Y falling (conditional):

Cell Name	**Input**	**When**	**Power(pJ)**		
			min	**mid**	**max**
INCL2W11OF2X1	**A**	**B**	0.01305	0.01322	0.02245
	B	**A**	0.01386	0.01419	0.02392

Passive power(pJ) for A rising (conditional):

Cell Name	**When**	**Power(pJ)**		
		min	**mid**	**max**
INCL2W11OF2X1	**B * !Y**	-0.00232	-0.00251	-0.00256
	!B * Y	-0.00279	-0.00280	-0.00280

Passive power(pJ) for A falling (conditional):

Cell Name	**When**	**Power(pJ)**		
		min	**mid**	**max**
INCL2W11OF2X1	**B * !Y**	0.00279	0.00280	0.00280
	!B * Y	0.00289	0.00284	0.00282

Passive power(pJ) for B rising (conditional):

Cell Name	**When**	**Power(pJ)**		
		min	**mid**	**max**
INCL2W11OF2X1	**A * !Y**	-0.00162	-0.00170	-0.00173
	!A * Y	-0.00201	-0.00201	-0.00202

Passive power(pJ) for B falling (conditional):

Cell Name	**When**	**Power(pJ)**		
		min	**mid**	**max**
INCL2W11OF2X1	**A * !Y**	0.00216	0.00217	0.00217
	!A * Y	0.00279	0.00274	0.00275

INCL2W11OF2X2

ASCEND_TSMC180_NCL_TT_1.80V_25C Cell Library: Process , Voltage 1.80, Temp 25.00

Truth Table

INPUT		OUTPUT
A	B	Y
0	x	1
1	0	1
1	1	0

Footprint

Cell Name	Area
INCL2W11OF2X2	39.9168

Pin Capacitance Information

Cell Name	Pin Cap(pf)		Max Cap(pf)
	A	B	Y
INCL2W11OF2X2	0.00373	0.00436	0.11865

Leakage Information

Cell Name	Leakage(nW)		
	Min.	Avg	Max.
INCL2W11OF2X2	0.03471	0.04969	0.07188

Delay Information

Delay(ns) to Y rising (conditional):

Cell Name	Timing Arc(Dir)	When	Delay(ns)		
			Min	Mid	Max
INCL2W11OF2X2	A->Y (FR)	!B	0.25632	0.32482	1.01196
	B->Y (FR)	!A	0.25689	0.34919	1.15359

Delay(ns) to Y falling (conditional):

Cell Name	Timing Arc(Dir)	When	Delay(ns)		
			Min	Mid	Max
INCL2W11OF2X2	A->Y (RF)	B	0.15340	0.19339	0.24011
	B->Y (RF)	A	0.15722	0.21140	0.31130

Power Information

Internal switching power(pJ) to Y rising (conditional):

Cell Name	Input	When	Power(pJ)		
			min	mid	max

INCL2W11OF2X2	**A**	**!B**	0.02475	0.02490	0.03819
	B	**!A**	0.02486	0.02510	0.03736

Internal switching power(pJ) to Y falling (conditional):

Cell Name	**Input**	**When**	**Power(pJ)**		
			min	**mid**	**max**
INCL2W11OF2X2	**A**	**B**	0.01886	0.01886	0.02860
	B	**A**	0.01959	0.01957	0.02966

Passive power(pJ) for A rising (conditional):

Cell Name	**When**	**Power(pJ)**		
		min	**mid**	**max**
INCL2W11OF2X2	**B * !Y**	-0.00206	-0.00224	-0.00231
	!B * Y	-0.00238	-0.00238	-0.00239

Passive power(pJ) for A falling (conditional):

Cell Name	**When**	**Power(pJ)**		
		min	**mid**	**max**
INCL2W11OF2X2	**B * !Y**	0.00258	0.00259	0.00260
	!B * Y	0.00250	0.00243	0.00242

Passive power(pJ) for B rising (conditional):

Cell Name	**When**	**Power(pJ)**		
		min	**mid**	**max**
INCL2W11OF2X2	**A * !Y**	-0.00169	-0.00183	-0.00189
	!A * Y	-0.00234	-0.00234	-0.00235

Passive power(pJ) for B falling (conditional):

Cell Name	**When**	**Power(pJ)**		
		min	**mid**	**max**
INCL2W11OF2X2	**A * !Y**	0.00233	0.00234	0.00234
	!A * Y	0.00299	0.00296	0.00296

INCL2W11OF2X4

ASCEND_TSMC180_NCL_TT_1.80V_25C Cell Library: Process , Voltage 1.80, Temp 25.00

Truth Table

INPUT		OUTPUT
A	B	Y
0	x	1
1	0	1
1	1	0

Footprint

Cell Name	Area
INCL2W11OF2X4	43.2432

Pin Capacitance Information

Cell Name	Pin Cap(pf)		Max Cap(pf)
	A	B	Y
INCL2W11OF2X4	0.00411	0.00433	0.11865

Leakage Information

Cell Name	Leakage(nW)		
	Min.	Avg	Max.
INCL2W11OF2X4	0.05243	0.07583	0.10625

Delay Information

Delay(ns) to Y rising (conditional):

Cell Name	Timing Arc(Dir)	When	Delay(ns)		
			Min	Mid	Max
INCL2W11OF2X4	A->Y (FR)	!B	0.24474	0.30471	0.83501
	B->Y (FR)	!A	0.24631	0.33000	0.98316

Delay(ns) to Y falling (conditional):

Cell Name	Timing Arc(Dir)	When	Delay(ns)		
			Min	Mid	Max
INCL2W11OF2X4	A->Y (RF)	B	0.15041	0.18764	0.17838
	B->Y (RF)	A	0.15321	0.20745	0.25530

Power Information

Internal switching power(pJ) to Y rising (conditional):

Cell Name	Input	When	Power(pJ)		
			min	mid	max

INCL2W11OF2X4	**A**	**!B**	0.03759	0.03773	0.05384
	B	**!A**	0.03712	0.03726	0.05333

Internal switching power(pJ) to Y falling (conditional):

Cell Name	**Input**	**When**	**Power(pJ)**		
			min	**mid**	**max**
INCL2W11OF2X4	**A**	**B**	0.02955	0.02952	0.04155
	B	**A**	0.03059	0.03077	0.04306

Passive power(pJ) for A rising (conditional):

Cell Name	**When**	**Power(pJ)**		
		min	**mid**	**max**
INCL2W11OF2X4	**B * !Y**	-0.00246	-0.00270	-0.00279
	!B * Y	-0.00284	-0.00284	-0.00285

Passive power(pJ) for A falling (conditional):

Cell Name	**When**	**Power(pJ)**		
		min	**mid**	**max**
INCL2W11OF2X4	**B * !Y**	0.00309	0.00309	0.00310
	!B * Y	0.00295	0.00289	0.00288

Passive power(pJ) for B rising (conditional):

Cell Name	**When**	**Power(pJ)**		
		min	**mid**	**max**
INCL2W11OF2X4	**A * !Y**	-0.00151	-0.00157	-0.00161
	!A * Y	-0.00227	-0.00227	-0.00228

Passive power(pJ) for B falling (conditional):

Cell Name	**When**	**Power(pJ)**		
		min	**mid**	**max**
INCL2W11OF2X4	**A * !Y**	0.00208	0.00208	0.00209
	!A * Y	0.00304	0.00300	0.00301

INCL3W111OF3X4

ASCEND_TSMC180_NCL_TT_1.80V_25C Cell Library: Process , Voltage 1.80, Temp 25.00

Truth Table

INPUT			OUTPUT
A	B	C	Y
0	x	x	1
1	0	x	1
1	1	0	1
1	1	1	0

Footprint

Cell Name	Area
INCL3W111OF3X4	49.8960

Pin Capacitance Information

Cell Name	Pin Cap(pf)			Max Cap(pf)
	A	B	C	Y
INCL3W111OF3X4	0.00705	0.00683	0.00710	0.11865

Leakage Information

Cell Name	Leakage(nW)		
	Min.	Avg	Max.
INCL3W111OF3X4	0.05365	0.07803	0.11186

Delay Information

Delay(ns) to Y rising (conditional):

Cell Name	Timing Arc(Dir)	When	Delay(ns)		
			Min	Mid	Max
INCL3W111OF3X4	A->Y (FR)	!B * !C	0.25721	0.29666	0.63534
	B->Y (FR)	!A * !C	0.25411	0.30892	0.77136
	C->Y (FR)	!A * !B	0.23699	0.31057	0.85919

Delay(ns) to Y falling (conditional):

Cell Name	Timing Arc(Dir)	When	Delay(ns)		
			Min	Mid	Max
INCL3W111OF3X4	A->Y (RF)	B * C	0.14591	0.16625	0.02421
	B->Y (RF)	A * C	0.14315	0.17422	0.06887
	C->Y (RF)	A * B	0.14149	0.18526	0.10988

Power Information

Internal switching power(pJ) to Y rising (conditional):

Cell Name	Input	When	Power(pJ)		
			min	mid	max
INCL3W111OF3X4	A	!B * !C	0.04591	0.04549	0.06509
	B	!A * !C	0.04428	0.04435	0.06365
	C	!A * !B	0.04255	0.04264	0.06245

Internal switching power(pJ) to Y falling (conditional):

Cell Name	Input	When	Power(pJ)		
			min	mid	max
INCL3W111OF3X4	A	B * C	0.02981	0.02936	0.04093
	B	A * C	0.03106	0.03121	0.04337
	C	A * B	0.03199	0.03210	0.04404

Passive power(pJ) for A rising (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
INCL3W111OF3X4	B * C * !Y	-0.00427	-0.00444	-0.00453
	B * !C * Y	-0.00472	-0.00475	-0.00476
	B * !C * !Y	-0.00472	-0.00474	-0.00474
	!B * C * Y	-0.00438	-0.00459	-0.00467
	!B * C * !Y	-0.00441	-0.00461	-0.00474
	!B * !C * Y	-0.00487	-0.00489	-0.00489

Passive power(pJ) for A falling (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
INCL3W111OF3X4	B * C * !Y	0.00468	0.00471	0.00473
	B * !C * Y	0.00478	0.00477	0.00476
	B * !C * !Y	0.00472	0.00474	0.00474
	!B * C * Y	0.00476	0.00468	0.00467
	!B * C * !Y	0.00621	0.00623	0.00624
	!B * !C * Y	0.00492	0.00492	0.00493

Passive power(pJ) for B rising (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
INCL3W111OF3X4	A * C * !Y	-0.00270	-0.00277	-0.00279
	A * !C * Y	-0.00416	-0.00416	-0.00416
	A * !C * !Y	-0.00323	-0.00325	-0.00325
	!A * C * Y	-0.00315	-0.00318	-0.00323
	!A * C * !Y	-0.00318	-0.00320	-0.00325
	!A * !C * Y	-0.00432	-0.00433	-0.00433

Passive power(pJ) for B falling (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
INCL3W111OF3X4	A * C * !Y	0.00286	0.00288	0.00288
	A * !C * Y	0.00430	0.00418	0.00416
	A * !C * !Y	0.00323	0.00325	0.00325
	!A * C * Y	0.00480	0.00484	0.00486
	!A * C * !Y	0.00444	0.00444	0.00444
	!A * !C * Y	0.00436	0.00435	0.00438

Passive power(pJ) for C rising (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
INCL3W111OF3X4	A * B * !Y	-0.00195	-0.00201	-0.00203
	A * !B * Y	-0.00289	-0.00305	-0.00327
	A * !B * !Y	-0.00289	-0.00305	-0.00326
	!A * B * Y	-0.00232	-0.00233	-0.00237
	!A * B * !Y	-0.00232	-0.00233	-0.00237
	!A * !B * Y	-0.00338	-0.00339	-0.00339

Passive power(pJ) for C falling (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
INCL3W111OF3X4	A * B * !Y	0.00297	0.00299	0.00297
	A * !B * Y	0.00452	0.00452	0.00452
	A * !B * !Y	0.00326	0.00326	0.00326
	!A * B * Y	0.00465	0.00467	0.00466
	!A * B * !Y	0.00292	0.00295	0.00293
	!A * !B * Y	0.00489	0.00485	0.00488

NCLP2W11OF2XL

ASCEND_TSMC180_NCL_TT_1.80V_25C Cell Library: Process , Voltage 1.80, Temp 25.00

Truth Table

INPUT		OUTPUT
A	B	Y
0	0	0
x	1	1
1	x	1

Footprint

Cell Name	Area
NCLP2W11OF2XL	39.9168

Pin Capacitance Information

Cell Name	Pin Cap(pf)		Max Cap(pf)
	A	B	Y
NCLP2W11OF2XL	0.00364	0.00432	0.11865

Leakage Information

Cell Name	Leakage(nW)		
	Min.	Avg	Max.
NCLP2W11OF2XL	0.02081	0.03973	0.04518

Delay Information

Delay(ns) to Y rising (conditional):

Cell Name	Timing Arc(Dir)	When	Delay(ns)		
			Min	Mid	Max
NCLP2W11OF2XL	A->Y (RR)	B	0.09222	0.16574	0.76116
	B->Y (RR)	A	0.09483	0.18423	0.83497

Delay(ns) to Y falling (conditional):

Cell Name	Timing Arc(Dir)	When	Delay(ns)		
			Min	Mid	Max
NCLP2W11OF2XL	A->Y (FF)	!B	0.21291	0.31258	1.16983
	B->Y (FF)	!A	0.21785	0.33905	1.31930

Power Information

Internal switching power(pJ) to Y rising (conditional):

Cell Name	Input	When	Power(pJ)		
			min	mid	max

NCLP2W11OF2XL	**A**	**B**	0.01057	0.01107	0.02097
	B	**A**	0.01137	0.01203	0.02231

Internal switching power(pJ) to Y falling (conditional):

Cell Name	Input	When	Power(pJ)		
			min	mid	max
NCLP2W11OF2XL	**A**	**!B**	0.02006	0.01971	0.03169
	B	**!A**	0.01999	0.01957	0.03066

Passive power(pJ) for A rising (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
NCLP2W11OF2XL	**B * Y**	-0.00213	-0.00231	-0.00236
	!B * !Y	-0.00239	-0.00239	-0.00240

Passive power(pJ) for A falling (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
NCLP2W11OF2XL	**B * Y**	0.00260	0.00260	0.00261
	!B * !Y	0.00249	0.00244	0.00242

Passive power(pJ) for B rising (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
NCLP2W11OF2XL	**A * Y**	-0.00145	-0.00151	-0.00154
	!A * !Y	-0.00202	-0.00203	-0.00203

Passive power(pJ) for B falling (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
NCLP2W11OF2XL	**A * Y**	0.00191	0.00191	0.00191
	!A * !Y	0.00278	0.00275	0.00277

NCLP2W11OF2X1

ASCEND_TSMC180_NCL_TT_1.80V_25C Cell Library: Process , Voltage 1.80, Temp 25.00

Truth Table

INPUT		OUTPUT
A	B	Y
0	0	0
x	1	1
1	x	1

Footprint

Cell Name	Area
NCLP2W11OF2X1	43.2432

Pin Capacitance Information

Cell Name	Pin Cap(pf)		Max Cap(pf)
	A	B	Y
NCLP2W11OF2X1	0.00448	0.00444	0.11865

Leakage Information

Cell Name	Leakage(nW)		
	Min.	Avg	Max.
NCLP2W11OF2X1	0.02446	0.04206	0.04882

Delay Information

Delay(ns) to Y rising (conditional):

Cell Name	Timing Arc(Dir)	When	Delay(ns)		
			Min	Mid	Max
NCLP2W11OF2X1	A->Y (RR)	B	0.10362	0.16854	0.57064
	B->Y (RR)	A	0.10354	0.18651	0.64527

Delay(ns) to Y falling (conditional):

Cell Name	Timing Arc(Dir)	When	Delay(ns)		
			Min	Mid	Max
NCLP2W11OF2X1	A->Y (FF)	!B	0.23445	0.32257	1.08440
	B->Y (FF)	!A	0.23261	0.34423	1.23498

Power Information

Internal switching power(pJ) to Y rising (conditional):

Cell Name	Input	When	Power(pJ)		
			min	mid	max

NCLP2W11OF2X1	**A**	**B**	0.01257	0.01299	0.02300
	B	**A**	0.01338	0.01416	0.02469

Internal switching power(pJ) to Y falling (conditional):

Cell Name	**Input**	**When**	**Power(pJ)**		
			min	**mid**	**max**
NCLP2W11OF2X1	**A**	**!B**	0.02382	0.02301	0.03522
	B	**!A**	0.02346	0.02268	0.03419

Passive power(pJ) for A rising (conditional):

Cell Name	**When**	**Power(pJ)**		
		min	**mid**	**max**
NCLP2W11OF2X1	**B * Y**	-0.00232	-0.00251	-0.00256
	!B * !Y	-0.00279	-0.00280	-0.00279

Passive power(pJ) for A falling (conditional):

Cell Name	**When**	**Power(pJ)**		
		min	**mid**	**max**
NCLP2W11OF2X1	**B * Y**	0.00279	0.00281	0.00280
	!B * !Y	0.00289	0.00283	0.00284

Passive power(pJ) for B rising (conditional):

Cell Name	**When**	**Power(pJ)**		
		min	**mid**	**max**
NCLP2W11OF2X1	**A * Y**	-0.00162	-0.00170	-0.00173
	!A * !Y	-0.00201	-0.00201	-0.00202

Passive power(pJ) for B falling (conditional):

Cell Name	**When**	**Power(pJ)**		
		min	**mid**	**max**
NCLP2W11OF2X1	**A * Y**	0.00216	0.00217	0.00217
	!A * !Y	0.00279	0.00274	0.00276

NCLP2W11OF2X2

ASCEND_TSMC180_NCL_TT_1.80V_25C Cell Library: Process , Voltage 1.80, Temp 25.00

Truth Table

INPUT		OUTPUT
A	B	Y
0	0	0
x	1	1
1	x	1

Footprint

Cell Name	Area
NCLP2W11OF2X2	36.5904

Pin Capacitance Information

Cell Name	Pin Cap(pf)		Max Cap(pf)
	A	B	Y
NCLP2W11OF2X2	0.00365	0.00417	0.11865

Leakage Information

Cell Name	Leakage(nW)		
	Min.	Avg	Max.
NCLP2W11OF2X2	0.02996	0.04846	0.05433

Delay Information

Delay(ns) to Y rising (conditional):

Cell Name	Timing Arc(Dir)	When	Delay(ns)		
			Min	Mid	Max
NCLP2W11OF2X2	A->Y (RR)	B	0.10565	0.15786	0.33738
	B->Y (RR)	A	0.10759	0.17802	0.41536

Delay(ns) to Y falling (conditional):

Cell Name	Timing Arc(Dir)	When	Delay(ns)		
			Min	Mid	Max
NCLP2W11OF2X2	A->Y (FF)	!B	0.27165	0.34514	0.99590
	B->Y (FF)	!A	0.27692	0.37113	1.15487

Power Information

Internal switching power(pJ) to Y rising (conditional):

Cell Name	Input	When	Power(pJ)		
			min	mid	max

NCLP2W11OF2X2	**A**	**B**	0.01584	0.01648	0.02766
	B	**A**	0.01665	0.01771	0.02937

Internal switching power(pJ) to Y falling (conditional):

Cell Name	**Input**	**When**	**Power(pJ)**		
			min	**mid**	**max**
NCLP2W11OF2X2	**A**	**!B**	0.03108	0.02935	0.03882
	B	**!A**	0.03105	0.02912	0.03819

Passive power(pJ) for A rising (conditional):

Cell Name	**When**	**Power(pJ)**		
		min	**mid**	**max**
NCLP2W11OF2X2	**B * Y**	-0.00206	-0.00222	-0.00227
	!B * !Y	-0.00237	-0.00237	-0.00238

Passive power(pJ) for A falling (conditional):

Cell Name	**When**	**Power(pJ)**		
		min	**mid**	**max**
NCLP2W11OF2X2	**B * Y**	0.00250	0.00250	0.00249
	!B * !Y	0.00248	0.00241	0.00240

Passive power(pJ) for B rising (conditional):

Cell Name	**When**	**Power(pJ)**		
		min	**mid**	**max**
NCLP2W11OF2X2	**A * Y**	-0.00140	-0.00147	-0.00148
	!A * !Y	-0.00194	-0.00194	-0.00194

Passive power(pJ) for B falling (conditional):

Cell Name	**When**	**Power(pJ)**		
		min	**mid**	**max**
NCLP2W11OF2X2	**A * Y**	0.00181	0.00181	0.00182
	!A * !Y	0.00261	0.00256	0.00257

NCLP2W11OF2X4

ASCEND_TSMC180_NCL_TT_1.80V_25C Cell Library: Process , Voltage 1.80, Temp 25.00

Truth Table

INPUT		OUTPUT
A	B	Y
0	0	0
x	1	1
1	x	1

Footprint

Cell Name	Area
NCLP2W11OF2X4	43.2432

Pin Capacitance Information

Cell Name	Pin Cap(pf)		Max Cap(pf)
	A	B	Y
NCLP2W11OF2X4	0.00409	0.00432	0.11865

Leakage Information

Cell Name	Leakage(nW)		
	Min.	Avg	Max.
NCLP2W11OF2X4	0.05084	0.07583	0.08634

Delay Information

Delay(ns) to Y rising (conditional):

Cell Name	Timing Arc(Dir)	When	Delay(ns)		
			Min	Mid	Max
NCLP2W11OF2X4	A->Y (RR)	B	0.15384	0.20545	0.33989
	B->Y (RR)	A	0.15700	0.22886	0.43400

Delay(ns) to Y falling (conditional):

Cell Name	Timing Arc(Dir)	When	Delay(ns)		
			Min	Mid	Max
NCLP2W11OF2X4	A->Y (FF)	!B	0.32122	0.38597	0.96077
	B->Y (FF)	!A	0.32495	0.41092	1.14250

Power Information

Internal switching power(pJ) to Y rising (conditional):

Cell Name	Input	When	Power(pJ)		
			min	mid	max

NCLP2W11OF2X4	**A**	**B**	0.03547	0.03499	0.05371
	B	**A**	0.03651	0.03649	0.05727

Internal switching power(pJ) to Y falling (conditional):

Cell Name	**Input**	**When**	**Power(pJ)**		
			min	**mid**	**max**
NCLP2W11OF2X4	**A**	**!B**	0.06747	0.06369	0.07056
	B	**!A**	0.06710	0.06328	0.07349

Passive power(pJ) for A rising (conditional):

Cell Name	**When**	**Power(pJ)**		
		min	**mid**	**max**
NCLP2W11OF2X4	**B * Y**	-0.00245	-0.00268	-0.00277
	!B * !Y	-0.00283	-0.00284	-0.00284

Passive power(pJ) for A falling (conditional):

Cell Name	**When**	**Power(pJ)**		
		min	**mid**	**max**
NCLP2W11OF2X4	**B * Y**	0.00308	0.00308	0.00309
	!B * !Y	0.00294	0.00287	0.00287

Passive power(pJ) for B rising (conditional):

Cell Name	**When**	**Power(pJ)**		
		min	**mid**	**max**
NCLP2W11OF2X4	**A * Y**	-0.00150	-0.00157	-0.00161
	!A * !Y	-0.00227	-0.00228	-0.00228

Passive power(pJ) for B falling (conditional):

Cell Name	**When**	**Power(pJ)**		
		min	**mid**	**max**
NCLP2W11OF2X4	**A * Y**	0.00208	0.00209	0.00209
	!A * !Y	0.00304	0.00301	0.00302

NCLP3W111OF3X4

ASCEND_TSMC180_NCL_TT_1.80V_25C Cell Library: Process , Voltage 1.80, Temp 25.00

Truth Table

INPUT			OUTPUT
A	B	C	Y
0	0	0	0
0	x	1	1
x	1	x	1
1	x	x	1

Footprint

Cell Name	Area
NCLP3W111OF3X4	49.8960

Pin Capacitance Information

Cell Name	Pin Cap(pf)			Max Cap(pf)
	A	B	C	Y
NCLP3W111OF3X4	0.00705	0.00688	0.00709	0.11865

Leakage Information

Cell Name	Leakage(nW)		
	Min.	Avg	Max.
NCLP3W111OF3X4	0.04441	0.07204	0.08690

Delay Information

Delay(ns) to Y rising (conditional):

Cell Name	Timing Arc(Dir)	When	Delay(ns)		
			Min	Mid	Max
NCLP3W111OF3X4	A->Y (RR)	B * C	0.11228	0.14139	0.10418
	B->Y (RR)	A * C	0.10957	0.15309	0.16146
	C->Y (RR)	A * B	0.10799	0.16759	0.21112

Delay(ns) to Y falling (conditional):

Cell Name	Timing Arc(Dir)	When	Delay(ns)		
			Min	Mid	Max
NCLP3W111OF3X4	A->Y (FF)	!B * !C	0.26710	0.31068	0.67015
	B->Y (FF)	!A * !C	0.26390	0.32332	0.81961
	C->Y (FF)	!A * !B	0.24830	0.32325	0.92070

Power Information

Internal switching power(pJ) to Y rising (conditional):

Cell Name	Input	When	Power(pJ)		
			min	mid	max
NCLP3W111OF3X4	A	B * C	0.02594	0.02618	0.04145
	B	A * C	0.02726	0.02850	0.04489
	C	A * B	0.02814	0.02957	0.04641

Internal switching power(pJ) to Y falling (conditional):

Cell Name	Input	When	Power(pJ)		
			min	mid	max
NCLP3W111OF3X4	A	!B * !C	0.05792	0.05528	0.06828
	B	!A * !C	0.05621	0.05415	0.06737
	C	!A * !B	0.05454	0.05215	0.06754

Passive power(pJ) for A rising (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
NCLP3W111OF3X4	B * C * Y	-0.00430	-0.00446	-0.00456
	B * !C * Y	-0.00475	-0.00476	-0.00477
	B * !C * !Y	-0.00475	-0.00478	-0.00476
	!B * C * Y	-0.00444	-0.00465	-0.00477
	!B * C * !Y	-0.00442	-0.00462	-0.00471
	!B * !C * !Y	-0.00490	-0.00492	-0.00492

Passive power(pJ) for A falling (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
NCLP3W111OF3X4	B * C * Y	0.00472	0.00475	0.00476
	B * !C * Y	0.00476	0.00476	0.00477
	B * !C * !Y	0.00480	0.00480	0.00476
	!B * C * Y	0.00624	0.00627	0.00628
	!B * C * !Y	0.00478	0.00471	0.00471
	!B * !C * !Y	0.00495	0.00494	0.00492

Passive power(pJ) for B rising (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
NCLP3W111OF3X4	A * C * Y	-0.00269	-0.00277	-0.00279
	A * !C * Y	-0.00322	-0.00325	-0.00324
	A * !C * !Y	-0.00417	-0.00418	-0.00416
	!A * C * Y	-0.00319	-0.00321	-0.00327
	!A * C * !Y	-0.00316	-0.00319	-0.00324
	!A * !C * !Y	-0.00433	-0.00434	-0.00434

Passive power(pJ) for B falling (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
NCLP3W111OF3X4	A * C * Y	0.00286	0.00287	0.00288
	A * !C * Y	0.00322	0.00325	0.00324
	A * !C * !Y	0.00430	0.00419	0.00416
	!A * C * Y	0.00443	0.00443	0.00445
	!A * C * !Y	0.00481	0.00485	0.00487
	!A * !C * !Y	0.00437	0.00435	0.00435

Passive power(pJ) for C rising (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
NCLP3W111OF3X4	A * B * Y	-0.00194	-0.00201	-0.00203
	A * !B * Y	-0.00291	-0.00307	-0.00325
	A * !B * !Y	-0.00291	-0.00307	-0.00326
	!A * B * Y	-0.00232	-0.00233	-0.00238
	!A * B * !Y	-0.00232	-0.00233	-0.00238
	!A * !B * !Y	-0.00338	-0.00338	-0.00340

Passive power(pJ) for C falling (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
NCLP3W111OF3X4	A * B * Y	0.00298	0.00297	0.00297
	A * !B * Y	0.00325	0.00327	0.00325
	A * !B * !Y	0.00453	0.00452	0.00453
	!A * B * Y	0.00291	0.00294	0.00292
	!A * B * !Y	0.00465	0.00466	0.00466
	!A * !B * !Y	0.00489	0.00485	0.00486

NCLP2W211OF3X4

ASCEND_TSMC180_NCL_TT_1.80V_25C Cell Library: Process , Voltage 1.80, Temp 25.00

Truth Table

INPUT			OUTPUT
A	B	C	Y
0	x	x	0
1	0	0	0
1	x	1	1
1	1	x	1

Footprint

Cell Name	Area
NCLP2W211OF3X4	49.8960

Pin Capacitance Information

Cell Name	Pin Cap(pf)			Max Cap(pf)
	A	B	C	Y
NCLP2W211OF3X4	0.00658	0.00624	0.00626	0.11865

Leakage Information

Cell Name	Leakage(nW)		
	Min.	Avg	Max.
NCLP2W211OF3X4	0.03736	0.06304	0.09364

Delay Information

Delay(ns) to Y rising (conditional):

Cell Name	Timing Arc(Dir)	When	Delay(ns)		
			Min	Mid	Max
NCLP2W211OF3X4	A->Y (RR)	B * C	0.15754	0.19418	0.45660
	B->Y (RR)	A * C	0.14720	0.19828	0.31149
	C->Y (RR)	A * B	0.14987	0.21701	0.37904

Delay(ns) to Y falling (conditional):

Cell Name	Timing Arc(Dir)	When	Delay(ns)		
			Min	Mid	Max
NCLP2W211OF3X4	A->Y (FF)	B * C	0.12170	0.21429	0.77805
	A->Y (FF)	B * !C	0.10668	0.19080	0.55736
	A->Y (FF)	!B * C	0.11330	0.19830	0.56653
	B->Y (FF)	A * !C	0.20329	0.26086	0.66127
	C->Y (FF)	A * !B	0.20101	0.28182	0.81950

Power Information

Internal switching power(pJ) to Y rising (conditional):

Cell Name	Input	When	Power(pJ)		
			min	mid	max
NCLP2W211OF3X4	A	B * C	0.03227	0.03211	0.06718
	B	A * C	0.03151	0.03140	0.04771
	C	A * B	0.03338	0.03349	0.05044

Internal switching power(pJ) to Y falling (conditional):

Cell Name	Input	When	Power(pJ)		
			min	mid	max
NCLP2W211OF3X4	A	B * C	0.04405	0.04633	0.08408
	A	B * !C	0.04070	0.04298	0.06620
	A	!B * C	0.04098	0.04279	0.06551
	B	A * !C	0.05031	0.04888	0.06548
	C	A * !B	0.04963	0.04826	0.06734

Passive power(pJ) for A rising (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
NCLP2W211OF3X4	B * !C * !Y	-0.00430	-0.00430	-0.00431
	!B * C * !Y	-0.00430	-0.00431	-0.00432
	!B * !C * !Y	-0.00430	-0.00431	-0.00433

Passive power(pJ) for A falling (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
NCLP2W211OF3X4	B * !C * !Y	0.00442	0.00434	0.00434
	!B * C * !Y	0.00439	0.00433	0.00434
	!B * !C * !Y	0.00462	0.00463	0.00462

Passive power(pJ) for B rising (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
NCLP2W211OF3X4	A * C * Y	-0.00346	-0.00376	-0.00385
	A * !C * !Y	-0.00411	-0.00415	-0.00415
	!A * C * !Y	-0.00344	-0.00348	-0.00351
	!A * !C * !Y	-0.00413	-0.00417	-0.00416

Passive power(pJ) for B falling (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
NCLP2W211OF3X4	A * C * Y	0.00406	0.00408	0.00408
	A * !C * !Y	0.00429	0.00418	0.00418

	!A * C * !Y	0.00447	0.00447	0.00446
	!A * !C * !Y	0.00487	0.00488	0.00495

Passive power(pJ) for C rising (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
NCLP2W211OF3X4	**A * B * Y**	-0.00212	-0.00221	-0.00223
	A * !B * !Y	-0.00349	-0.00350	-0.00349
	!A * B * !Y	-0.00106	-0.00106	-0.00112
	!A * !B * !Y	-0.00352	-0.00353	-0.00355

Passive power(pJ) for C falling (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
NCLP2W211OF3X4	**A * B * Y**	0.00334	0.00335	0.00334
	A * !B * !Y	0.00462	0.00459	0.00461
	!A * B * !Y	0.00459	0.00460	0.00462
	!A * !B * !Y	0.00459	0.00458	0.00463

NCLP3W211OF3X4

ASCEND_TSMC180_NCL_TT_1.80V_25C Cell Library: Process , Voltage 1.80, Temp 25.00

Truth Table

INPUT			OUTPUT
A	B	C	Y
0	0	x	0
0	1	0	0
x	1	1	1
1	x	x	1

Footprint

Cell Name	Area
NCLP3W211OF3X4	49.8960

Pin Capacitance Information

Cell Name	Pin Cap(pf)			Max Cap(pf)
	A	B	C	Y
NCLP3W211OF3X4	0.00529	0.00587	0.00588	0.11865

Leakage Information

Cell Name	Leakage(nW)		
	Min.	Avg	Max.
NCLP3W211OF3X4	0.04089	0.06673	0.08253

Delay Information

Delay(ns) to Y rising (conditional):

Cell Name	Timing Arc(Dir)	When	Delay(ns)		
			Min	Mid	Max
NCLP3W211OF3X4	A->Y (RR)	B * C	0.10961	0.16983	0.23759
	B->Y (RR)	A * C	0.11345	0.15913	0.19073
	C->Y (RR)	A * B	0.11712	0.14734	0.12953

Delay(ns) to Y falling (conditional):

Cell Name	Timing Arc(Dir)	When	Delay(ns)		
			Min	Mid	Max
NCLP3W211OF3X4	A->Y (FF)	B * !C	0.36950	0.45376	1.21796
	A->Y (FF)	!B * C	0.35439	0.43485	1.18936
	A->Y (FF)	!B * !C	0.27416	0.35970	1.06109
	B->Y (FF)	!A * C	0.36074	0.42164	0.98046
	C->Y (FF)	!A * B	0.37177	0.43558	1.01659

Power Information

Internal switching power(pJ) to Y rising (conditional):

Cell Name	Input	When	Power(pJ)		
			min	mid	max
NCLP3W211OF3X4	A	B * C	0.02841	0.03010	0.04741
	B	A * C	0.02759	0.02859	0.04515
	C	A * B	0.02759	0.02793	0.04306

Internal switching power(pJ) to Y falling (conditional):

Cell Name	Input	When	Power(pJ)		
			min	mid	max
NCLP3W211OF3X4	A	B * !C	0.06472	0.06106	0.06594
	A	!B * C	0.06333	0.05947	0.06492
	A	!B * !C	0.05525	0.05218	0.06304
	B	!A * C	0.06330	0.05940	0.06173
	C	!A * B	0.06462	0.06084	0.06332

Passive power(pJ) for A rising (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
NCLP3W211OF3X4	B * C * Y	-0.00182	-0.00190	-0.00191
	B * !C * !Y	0.00115	0.00115	0.00115
	!B * C * !Y	-0.00174	-0.00175	-0.00175
	!B * !C * !Y	-0.00179	-0.00179	-0.00180

Passive power(pJ) for A falling (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
NCLP3W211OF3X4	B * C * Y	0.00328	0.00328	0.00329
	B * !C * !Y	0.00316	0.00315	0.00315
	!B * C * !Y	0.00316	0.00314	0.00314
	!B * !C * !Y	0.00316	0.00314	0.00312

Passive power(pJ) for B rising (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
NCLP3W211OF3X4	A * C * Y	-0.00224	-0.00238	-0.00244
	A * !C * Y	-0.00189	-0.00190	-0.00190
	A * !C * !Y	-0.00187	-0.00187	-0.00187
	!A * C * !Y	-0.00280	-0.00280	-0.00281
	!A * !C * !Y	-0.00284	-0.00284	-0.00284

Passive power(pJ) for B falling (conditional):

		Power(pJ)

Cell Name	When	min	mid	max
NCLP3W211OF3X4	A * C * Y	0.00268	0.00268	0.00269
	A * !C * Y	0.00252	0.00252	0.00253
	A * !C * !Y	0.00345	0.00344	0.00345
	!A * C * !Y	0.00310	0.00286	0.00283
	!A * !C * !Y	0.00423	0.00426	0.00435

Passive power(pJ) for C rising (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
NCLP3W211OF3X4	A * B * Y	-0.00228	-0.00243	-0.00249
	A * !B * Y	-0.00257	-0.00257	-0.00259
	A * !B * !Y	-0.00280	-0.00280	-0.00281
	!A * B * !Y	-0.00289	-0.00289	-0.00290
	!A * !B * !Y	-0.00289	-0.00290	-0.00291

Passive power(pJ) for C falling (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
NCLP3W211OF3X4	A * B * Y	0.00273	0.00273	0.00274
	A * !B * Y	0.00257	0.00257	0.00259
	A * !B * !Y	0.00306	0.00301	0.00301
	!A * B * !Y	0.00295	0.00292	0.00292
	!A * !B * !Y	0.00290	0.00291	0.00292

INCLP2W11OF2XL

ASCEND_TSMC180_NCL_TT_1.80V_25C Cell Library: Process , Voltage 1.80, Temp 25.00

Truth Table

INPUT		OUTPUT
A	B	Y
0	0	1
x	1	0
1	x	0

Footprint

Cell Name	Area
INCLP2W11OF2XL	39.9168

Pin Capacitance Information

Cell Name	Pin Cap(pf)		Max Cap(pf)
	A	B	Y
INCLP2W11OF2XL	0.00352	0.00414	0.11865

Leakage Information

Cell Name	Leakage(nW)		
	Min.	Avg	Max.
INCLP2W11OF2XL	0.02529	0.03970	0.06143

Delay Information

Delay(ns) to Y rising (conditional):

Cell Name	Timing Arc(Dir)	When	Delay(ns)		
			Min	Mid	Max
INCLP2W11OF2XL	A->Y (FR)	!B	0.22777	0.31867	1.44950
	B->Y (FR)	!A	0.23060	0.34585	1.58760

Delay(ns) to Y falling (conditional):

Cell Name	Timing Arc(Dir)	When	Delay(ns)		
			Min	Mid	Max
INCLP2W11OF2XL	A->Y (RF)	B	0.14945	0.20328	0.46920
	B->Y (RF)	A	0.15164	0.21828	0.53427

Power Information

Internal switching power(pJ) to Y rising (conditional):

Cell Name	Input	When	Power(pJ)		
			min	mid	max

INCLP2W11OF2XL	**A**	**!B**	0.01726	0.01764	0.03046
	B	**!A**	0.01710	0.01753	0.02915

Internal switching power(pJ) to Y falling (conditional):

Cell Name	Input	When	Power(pJ)		
			min	mid	max
INCLP2W11OF2XL	**A**	**B**	0.01085	0.01116	0.02008
	B	**A**	0.01164	0.01196	0.02119

Passive power(pJ) for A rising (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
INCLP2W11OF2XL	**B * !Y**	-0.00208	-0.00225	-0.00230
	!B * Y	-0.00234	-0.00234	-0.00235

Passive power(pJ) for A falling (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
INCLP2W11OF2XL	**B * !Y**	0.00254	0.00254	0.00254
	!B * Y	0.00244	0.00239	0.00237

Passive power(pJ) for B rising (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
INCLP2W11OF2XL	**A * !Y**	-0.00141	-0.00148	-0.00149
	!A * Y	-0.00193	-0.00192	-0.00193

Passive power(pJ) for B falling (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
INCLP2W11OF2XL	**A * !Y**	0.00184	0.00185	0.00186
	!A * Y	0.00270	0.00265	0.00266

INCLP2W11OF2X1

ASCEND_TSMC180_NCL_TT_1.80V_25C Cell Library: Process , Voltage 1.80, Temp 25.00

Truth Table

INPUT		OUTPUT
A	B	Y
0	0	1
x	1	0
1	x	0

Footprint

Cell Name	Area
INCLP2W11OF2X1	43.2432

Pin Capacitance Information

Cell Name	Pin Cap(pf)		Max Cap(pf)
	A	B	Y
INCLP2W11OF2X1	0.00453	0.00444	0.11865

Leakage Information

Cell Name	Leakage(nW)		
	Min.	Avg	Max.
INCLP2W11OF2X1	0.02763	0.04206	0.06376

Delay Information

Delay(ns) to Y rising (conditional):

Cell Name	Timing Arc(Dir)	When	Delay(ns)		
			Min	Mid	Max
INCLP2W11OF2X1	A->Y (FR)	!B	0.25205	0.33116	1.26079
	B->Y (FR)	!A	0.24938	0.35372	1.40217

Delay(ns) to Y falling (conditional):

Cell Name	Timing Arc(Dir)	When	Delay(ns)		
			Min	Mid	Max
INCLP2W11OF2X1	A->Y (RF)	B	0.14536	0.19300	0.36799
	B->Y (RF)	A	0.14519	0.20846	0.43703

Power Information

Internal switching power(pJ) to Y rising (conditional):

Cell Name	Input	When	Power(pJ)		
			min	mid	max

INCLP2W11OF2X1	**A**	**!B**	0.02045	0.02071	0.03416
	B	**!A**	0.02006	0.02040	0.03276

Internal switching power(pJ) to Y falling (conditional):

Cell Name	**Input**	**When**	**Power(pJ)**		
			min	**mid**	**max**
INCLP2W11OF2X1	**A**	**B**	0.01305	0.01322	0.02245
	B	**A**	0.01386	0.01419	0.02392

Passive power(pJ) for A rising (conditional):

Cell Name	**When**	**Power(pJ)**		
		min	**mid**	**max**
INCLP2W11OF2X1	**B * !Y**	-0.00232	-0.00251	-0.00256
	!B * Y	-0.00279	-0.00280	-0.00280

Passive power(pJ) for A falling (conditional):

Cell Name	**When**	**Power(pJ)**		
		min	**mid**	**max**
INCLP2W11OF2X1	**B * !Y**	0.00279	0.00280	0.00280
	!B * Y	0.00289	0.00284	0.00282

Passive power(pJ) for B rising (conditional):

Cell Name	**When**	**Power(pJ)**		
		min	**mid**	**max**
INCLP2W11OF2X1	**A * !Y**	-0.00162	-0.00170	-0.00173
	!A * Y	-0.00201	-0.00201	-0.00202

Passive power(pJ) for B falling (conditional):

Cell Name	**When**	**Power(pJ)**		
		min	**mid**	**max**
INCLP2W11OF2X1	**A * !Y**	0.00216	0.00217	0.00217
	!A * Y	0.00279	0.00274	0.00275

INCLP2W11OF2X2

ASCEND_TSMC180_NCL_TT_1.80V_25C Cell Library: Process , Voltage 1.80, Temp 25.00

Truth Table

INPUT		OUTPUT
A	B	Y
0	0	1
x	1	0
1	x	0

Footprint

Cell Name	Area
INCLP2W11OF2X2	39.9168

Pin Capacitance Information

Cell Name	Pin Cap(pf)		Max Cap(pf)
	A	B	Y
INCLP2W11OF2X2	0.00373	0.00436	0.11865

Leakage Information

Cell Name	Leakage(nW)		
	Min.	Avg	Max.
INCLP2W11OF2X2	0.03471	0.04969	0.07188

Delay Information

Delay(ns) to Y rising (conditional):

Cell Name	Timing Arc(Dir)	When	Delay(ns)		
			Min	Mid	Max
INCLP2W11OF2X2	A->Y (FR)	!B	0.25632	0.32482	1.01196
	B->Y (FR)	!A	0.25689	0.34919	1.15359

Delay(ns) to Y falling (conditional):

Cell Name	Timing Arc(Dir)	When	Delay(ns)		
			Min	Mid	Max
INCLP2W11OF2X2	A->Y (RF)	B	0.15340	0.19339	0.24011
	B->Y (RF)	A	0.15722	0.21140	0.31130

Power Information

Internal switching power(pJ) to Y rising (conditional):

Cell Name	Input	When	Power(pJ)		
			min	mid	max

INCLP2W11OF2X2	**A**	**!B**	0.02475	0.02490	0.03819
	B	**!A**	0.02486	0.02510	0.03736

Internal switching power(pJ) to Y falling (conditional):

Cell Name	Input	When	Power(pJ)		
			min	mid	max
INCLP2W11OF2X2	**A**	**B**	0.01886	0.01886	0.02860
	B	**A**	0.01959	0.01957	0.02966

Passive power(pJ) for A rising (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
INCLP2W11OF2X2	**B * !Y**	-0.00206	-0.00224	-0.00231
	!B * Y	-0.00238	-0.00238	-0.00239

Passive power(pJ) for A falling (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
INCLP2W11OF2X2	**B * !Y**	0.00258	0.00259	0.00260
	!B * Y	0.00250	0.00243	0.00242

Passive power(pJ) for B rising (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
INCLP2W11OF2X2	**A * !Y**	-0.00169	-0.00183	-0.00189
	!A * Y	-0.00234	-0.00234	-0.00235

Passive power(pJ) for B falling (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
INCLP2W11OF2X2	**A * !Y**	0.00233	0.00234	0.00234
	!A * Y	0.00299	0.00296	0.00296

INCLP2W11OF2X4

ASCEND_TSMC180_NCL_TT_1.80V_25C Cell Library: Process , Voltage 1.80, Temp 25.00

Truth Table

INPUT		OUTPUT
A	B	Y
0	0	1
x	1	0
1	x	0

Footprint

Cell Name	Area
INCLP2W11OF2X4	43.2432

Pin Capacitance Information

Cell Name	Pin Cap(pf)		Max Cap(pf)
	A	B	Y
INCLP2W11OF2X4	0.00411	0.00433	0.11865

Leakage Information

Cell Name	Leakage(nW)		
	Min.	Avg	Max.
INCLP2W11OF2X4	0.05243	0.07583	0.10625

Delay Information

Delay(ns) to Y rising (conditional):

Cell Name	Timing Arc(Dir)	When	Delay(ns)		
			Min	Mid	Max
INCLP2W11OF2X4	A->Y (FR)	!B	0.24474	0.30471	0.83501
	B->Y (FR)	!A	0.24631	0.33000	0.98316

Delay(ns) to Y falling (conditional):

Cell Name	Timing Arc(Dir)	When	Delay(ns)		
			Min	Mid	Max
INCLP2W11OF2X4	A->Y (RF)	B	0.15041	0.18764	0.17838
	B->Y (RF)	A	0.15321	0.20745	0.25530

Power Information

Internal switching power(pJ) to Y rising (conditional):

Cell Name	Input	When	Power(pJ)		
			min	mid	max

INCLP2W11OF2X4	**A**	**!B**	0.03759	0.03773	0.05384
	B	**!A**	0.03712	0.03726	0.05333

Internal switching power(pJ) to Y falling (conditional):

Cell Name	**Input**	**When**	**Power(pJ)**		
			min	**mid**	**max**
INCLP2W11OF2X4	**A**	**B**	0.02955	0.02952	0.04155
	B	**A**	0.03059	0.03077	0.04306

Passive power(pJ) for A rising (conditional):

Cell Name	**When**	**Power(pJ)**		
		min	**mid**	**max**
INCLP2W11OF2X4	**B * !Y**	-0.00246	-0.00270	-0.00279
	!B * Y	-0.00284	-0.00284	-0.00285

Passive power(pJ) for A falling (conditional):

Cell Name	**When**	**Power(pJ)**		
		min	**mid**	**max**
INCLP2W11OF2X4	**B * !Y**	0.00309	0.00309	0.00310
	!B * Y	0.00295	0.00289	0.00288

Passive power(pJ) for B rising (conditional):

Cell Name	**When**	**Power(pJ)**		
		min	**mid**	**max**
INCLP2W11OF2X4	**A * !Y**	-0.00151	-0.00157	-0.00161
	!A * Y	-0.00227	-0.00227	-0.00228

Passive power(pJ) for B falling (conditional):

Cell Name	**When**	**Power(pJ)**		
		min	**mid**	**max**
INCLP2W11OF2X4	**A * !Y**	0.00208	0.00208	0.00209
	!A * Y	0.00304	0.00300	0.00301

INCLP3W111OF3X4

ASCEND_TSMC180_NCL_TT_1.80V_25C Cell Library: Process , Voltage 1.80, Temp 25.00

Truth Table

INPUT			OUTPUT
A	B	C	Y
0	0	0	1
0	x	1	0
x	1	x	0
1	x	x	0

Footprint

Cell Name	Area
INCLP3W111OF3X4	49.8960

Pin Capacitance Information

Cell Name	Pin Cap(pf)			Max Cap(pf)
	A	B	C	Y
INCLP3W111OF3X4	0.00705	0.00683	0.00710	0.11865

Leakage Information

Cell Name	Leakage(nW)		
	Min.	Avg	Max.
INCLP3W111OF3X4	0.05365	0.07803	0.11186

Delay Information

Delay(ns) to Y rising (conditional):

Cell Name	Timing Arc(Dir)	When	Delay(ns)		
			Min	Mid	Max
INCLP3W111OF3X4	A->Y (FR)	!B * !C	0.25721	0.29666	0.63534
	B->Y (FR)	!A * !C	0.25411	0.30892	0.77136
	C->Y (FR)	!A * !B	0.23699	0.31057	0.85919

Delay(ns) to Y falling (conditional):

Cell Name	Timing Arc(Dir)	When	Delay(ns)		
			Min	Mid	Max
INCLP3W111OF3X4	A->Y (RF)	B * C	0.14591	0.16625	0.02421
	B->Y (RF)	A * C	0.14315	0.17422	0.06887
	C->Y (RF)	A * B	0.14149	0.18526	0.10988

Power Information

Internal switching power(pJ) to Y rising (conditional):

Cell Name	Input	When	Power(pJ)		
			min	mid	max
INCLP3W111OF3X4	A	!B * !C	0.04591	0.04549	0.06509
	B	!A * !C	0.04428	0.04435	0.06365
	C	!A * !B	0.04255	0.04264	0.06245

Internal switching power(pJ) to Y falling (conditional):

Cell Name	Input	When	Power(pJ)		
			min	mid	max
INCLP3W111OF3X4	A	B * C	0.02981	0.02936	0.04093
	B	A * C	0.03106	0.03121	0.04337
	C	A * B	0.03199	0.03210	0.04404

Passive power(pJ) for A rising (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
INCLP3W111OF3X4	B * C * !Y	-0.00427	-0.00444	-0.00453
	B * !C * Y	-0.00472	-0.00475	-0.00476
	B * !C * !Y	-0.00472	-0.00474	-0.00474
	!B * C * Y	-0.00438	-0.00459	-0.00467
	!B * C * !Y	-0.00441	-0.00461	-0.00474
	!B * !C * Y	-0.00487	-0.00489	-0.00489

Passive power(pJ) for A falling (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
INCLP3W111OF3X4	B * C * !Y	0.00468	0.00471	0.00473
	B * !C * Y	0.00478	0.00477	0.00476
	B * !C * !Y	0.00472	0.00474	0.00474
	!B * C * Y	0.00476	0.00468	0.00467
	!B * C * !Y	0.00621	0.00623	0.00624
	!B * !C * Y	0.00492	0.00492	0.00493

Passive power(pJ) for B rising (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
INCLP3W111OF3X4	A * C * !Y	-0.00270	-0.00277	-0.00279
	A * !C * Y	-0.00416	-0.00416	-0.00416
	A * !C * !Y	-0.00323	-0.00325	-0.00325
	!A * C * Y	-0.00315	-0.00318	-0.00323
	!A * C * !Y	-0.00318	-0.00320	-0.00325
	!A * !C * Y	-0.00432	-0.00433	-0.00433

Passive power(pJ) for B falling (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
INCLP3W111OF3X4	A * C * !Y	0.00286	0.00288	0.00288
	A * !C * Y	0.00430	0.00418	0.00416
	A * !C * !Y	0.00323	0.00325	0.00325
	!A * C * Y	0.00480	0.00484	0.00486
	!A * C * !Y	0.00444	0.00444	0.00444
	!A * !C * Y	0.00436	0.00435	0.00438

Passive power(pJ) for C rising (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
INCLP3W111OF3X4	A * B * !Y	-0.00195	-0.00201	-0.00203
	A * !B * Y	-0.00289	-0.00305	-0.00327
	A * !B * !Y	-0.00289	-0.00305	-0.00326
	!A * B * Y	-0.00232	-0.00233	-0.00237
	!A * B * !Y	-0.00232	-0.00233	-0.00237
	!A * !B * Y	-0.00338	-0.00339	-0.00339

Passive power(pJ) for C falling (conditional):

Cell Name	When	Power(pJ)		
		min	mid	max
INCLP3W111OF3X4	A * B * !Y	0.00297	0.00299	0.00297
	A * !B * Y	0.00452	0.00452	0.00452
	A * !B * !Y	0.00326	0.00326	0.00326
	!A * B * Y	0.00465	0.00467	0.00466
	!A * B * !Y	0.00292	0.00295	0.00293
	!A * !B * Y	0.00489	0.00485	0.00488