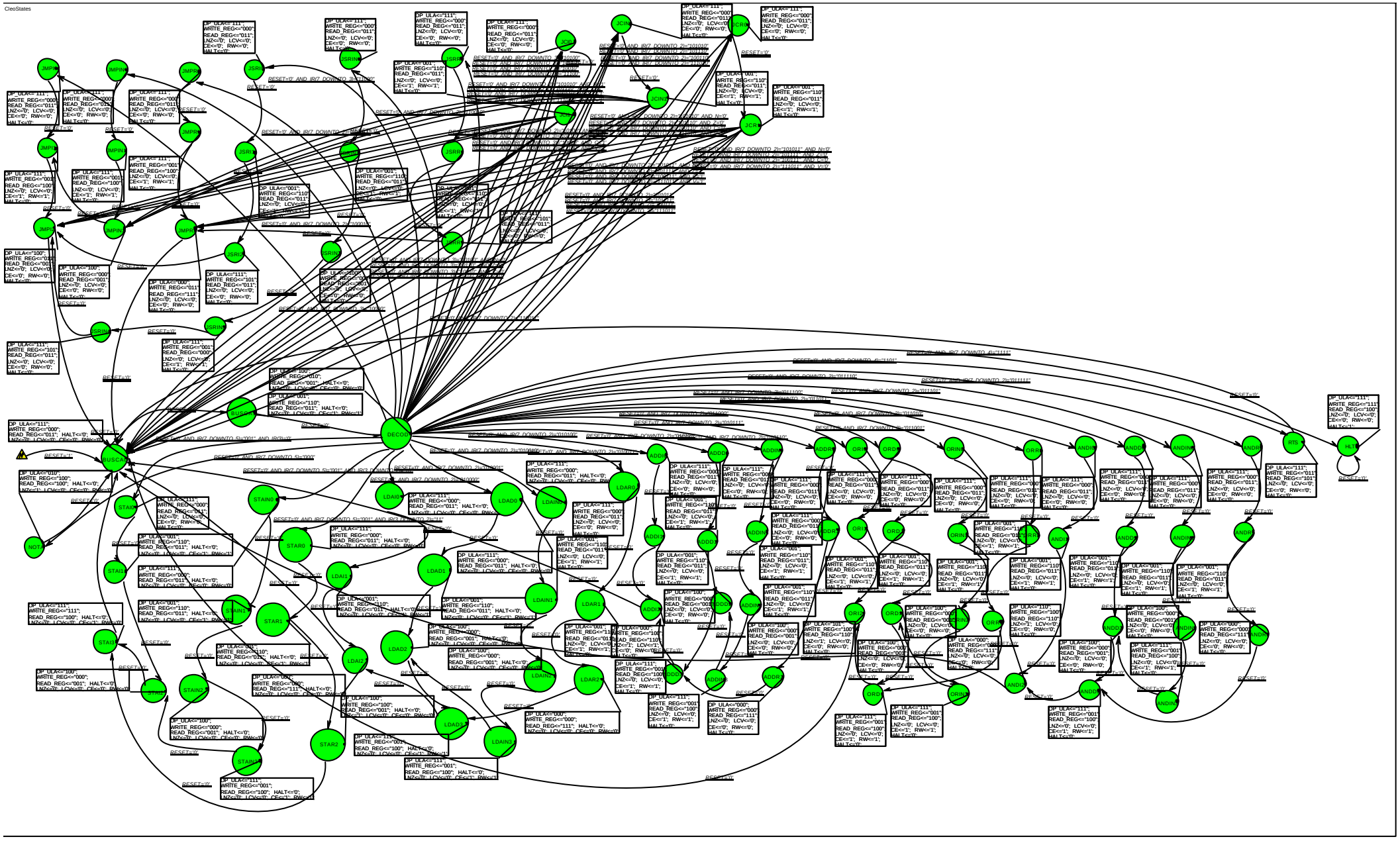
Diagram ACTIONS

Architecture: CleoBCfsm_arch

IR[7:2]
reset
clock
V
Z
N
C
READ_REG[2:0]
WRITE_REG[2:0]
OP_ULA[2:0]
LNZ
RW
CE
HALT